Annalisa Massini

Curriculum Vitae

"Ma, soprattutto, bisognerebbe imparare a dubitare, a diventare scettici." - Margherita Hack

Appointments

2001–today **Associate Professor**, INF01, Computer Science Department - *Sapienza* University of Rome.
1st november 2001

1996–2001 **Researcher**, K05B, Computer Science Department - *Sapienza* University of Rome.
8th January 1996 - 31st October 2001

Education

1993 **PhD in Computer Science**, V cycle, Computer Science Department - University of Rome *La Sapienza*, PhD thesis: *High efficiency self-routing interconnection networks*.
Supervisor Prof. G. A. De Biase

1989 **Laurea degree in Mathematics**, University of Rome *La Sapienza*, Thesis: *Binary redundant number representation for a parallel arithmetic on optical and electronic computers*.
Supervisor Prof. G. A. De Biase

Scholarship

1994-1996 **PostDoc Scholarship**, Computer Science Department - University of Rome *La Sapienza*.

1993-1994 **Scholarship**, Hewlett Packard, realization of a prototype for Information Appliance.

1993-1994 **Scholarship**, National Research Counsil (CNR), n. 201.12.61 - 21/7/89 for Focused Project *Sistemi Informatici e Calcolo Parallelo* on the topic *Design of HW modules for numerical signal processing elaboration - Studio e progetto di moduli HW per l'elaborazione numerica di segnali*.
overlapping with the PhD Scholarship - not accepted

Research interests

Research interests include: system level verification, mobile sensor networks, GPU based simulations, parallel architecture and parallel arithmetic units, interconnection networks.

Projects participation

European Projects

2013–2016 FP7-ICT-2011-9 - ICT-2011.5.2 – PAEON – *Project Title:* Model Driven Computation of Treatments for Infertility Related Endocrinological Diseases *Project Duration:* 36 Months, 01/02/2013 – 31/01/2016 **Task responsible** per il task T1.2 – Project Monitoring

2012–2015 FP7-ICT-2011-8 - ICT-2011.6.1 – SMARTHG – *Project Title:* Energy Demand Aware Open Services for Smart Grid Intelligent Automation *Project Duration:* 36 Months, 01/10/2012 – 30/09/2015 **Task responsible** per il task T1.3 – Quality Assurance

National projects

2009–2011 MIUR PRIN 2008 "Autonomic Security" - **Participant**

2006–2012 Project under the MIUR Program (Art. 12 del Decreto Ministeriale 8 agosto 2000 n. 593 - Bando Aerospazio Lazio) Title: Integrated system for managment and control of TRAnsport of Dangerous Materials - TRAMP (DM 24283) **Responsible for the managment of training activities and for the Project reporting** Teacher of the Computer Networks course

Teaching

Digital System Design, *Bachelor degree in Computer Science*, Sapienza University of Rome.
2008/09 - today

Intensive Computation, *Master degree in Computer Science/*, Sapienza University of Rome.
2007/08 - today

Computer Architecture, *Bachelor degree in Computer Science*, Sapienza University of Rome.
2008/09 - 2010/11

Advanced Parallel Architectures, *Master degree in Computer Science*, Sapienza University of Rome.
2014/2015 and 2016/2017

Computer Architecture III module A and module B, *Master degree in Computer Science*, Sapienza University of Rome.
2009/10

Informatics, *Specialization School in Medical Physics, Sapienza University of Rome*, Matlab programming. Image processing.
2009/2010 - today

Computer Networks, *Prog. MIUR TRAMP - 50 hours.*
2008-09

Computer Architecture - I module, *Degree in Computer Science*, Sapienza University of Rome.
2001/02 - 2007/08

Computer Architecture - II module, *Degree in Computer Science*, Sapienza University of Rome.
2001/02 - 2007/08

Computer Architecture Lab, *Degree in Computer Science*, Sapienza University of Rome.
1997/98 - 2000/01

Teaching assistant for Computer architecture , *Degree in Computer Science*, Sapienza University of Rome.
1997/98 - 2000/01

Maternity leave

Mandatory maternity leave from 16/5/2003 to 16/10/2003

Mandatory maternity leave from 30/4/2001 to 30/9/2001

Mandatory maternity leave from 22/10/1997 to 26/3/1998

Mandatory maternity leave from 7/2/1996 to 7/7/1996

Institutional activities

Department and Faculty

1996–today	Computer Science Department member
2019–today	Member of the committee for teaching and research activities of the graduate and undergraduate program
2014–today	Elected member of the department board as representative of the associate professors for the departmnet and the Faculty (I3S)
2011–today	UGOV responsible for the Computer Science Department
2011–today	VQR responsible for the Computer Science Department
2009–2010	Member of the evaluation committee for the bachelor degree programs in computer science
2004-2007	Member of the committee for the transfer to the bachelor degree programs in computer science

PhD school

2001-today	Member of the PhD Faculty board
2019	Member of the PhD admission committee in Computer Science Program (XXXV cycle) Sapienza University of Rome
2010	Member of the PhD admission committee in Computer Science Program (XXVI cycle) Sapienza University of Rome
2006	Chair of the PhD admission committee in Computer Science Program (XXII cycle) Sapienza University of Rome

Journal papers

R1 N. Bartolini, T. He, V. Arrigoni, A. Massini, F. Trombetti, H. Khamfroush *On Fundamental Bounds on Failure Identifiability by Boolean Network Tomography*, IEEE Transactions on Networking, to appear, 2020

R2 S. Gioiosa, M. Bolis, T. Flati, A. Massini, E. Garattini, G. Chillemi, M. Fratelli, T. Castrignanò *Massive NGS data analysis reveals hundreds of potential novel gene fusions in human cell lines*, GigaScience, 7(10), 1-8, 2018

R3 T. Mancini, A. Massini, E. Tronci *Parallelization of Cycle-Based Logic Simulation*, Parallel Processing Letters 27(2): 1-16, 2017

R4 T. Mancini, F. Mari, A. Massini, I. Melatti, I. Salvo, E. Tronci *On minimising the maximum expected verification time*, Information Processing Letters, 122, 1, 8-16, 2017

R5 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *SyLVaaS: System Level Formal Verification as a Service*, Fundamenta Informaticae 149(1-2): 101-132, 2016

R6 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *Anytime system level verification via parallel random exhaustive hardware in the loop simulation*, Microprocessors and Microsystems - Embedded Hardware Design 41: 12-28, 2016

R7 N. Bartolini, A. Massini, S. Silvestri *P&P: an asynchronous and distributed protocol for mobile sensor deployment*, Wireless Networks, 18(4), 381-399, 2012

R8 N. Bartolini, T. Calamoneri, A. Massini, S. Silvestri *On adaptive density deployment to mitigate the sink hole problem in mobile sensor networks*, ACM Springer Mobile Networks and Applications, 16:134-145, 2011

R9 N.Bartolini, T. Calamoneri. E. G. Fusco, A. Massini, S. Silvestri *Push and Pull: Autonomous Deployment of Mobile Sensors for a Complete Coverage* Wireless Networks, 16(3), 607 - 625, 2010

R10 T. Calamoneri, A. Massini, L. Torok, I. Vrto *Antibandwidth of Complete k-ary Trees* Discrete Mathematics, Vol. 309, No. 22, 6408-6414, 2009

R11 T. Calamoneri, A. Massini *Nearly Optimal Three Dimensional Layout of Hypercubes* Networks, 47(19), pp. 1-8, 2006

R12 T. Calamoneri, A. Massini Efficient *Algorithms for Checking the Equivalence of Multistage Interconnection Networks* Journal of Parallel and Distributed Computing, 64, 135 - 150, 2004

R13 T. Calamoneri , A. Massini, I. Vrto *New results on Edge-Bandwidth* Theoretical Computer Science, 307, 503-513, 2003

R14 A. Massini *All-to-all personalized communication on multistage interconnection networks* Discrete Applied Mathematics, 128, 435-446, 2003

R15 T. Calamoneri, A. Massini *Optimal Three-Dimensional Layout of Interconnection Networks* Theoretical Computer Science, 255, 263-279, 2001

R16 G. Bongiovanni, G. A. De Biase, A. Massini, A. Monti *The shuffled mesh a flexible and efficient model for parallel computing* Telecommunication Systems, Vol 13-1, 21-27, 2000

R17 T. Calamoneri, A. Massini *An Optimal Layout of Multigrid Networks* Information Processing Letters, 72, 137-141, 1999

R18 G. A. De Biase, A. Massini *A virtually nonblocking self-routing permutation network which routes packets in O($log_2 N$)* Telecommunication Systems, 10, 135-147, 1998

R19 G. A. De Biase, C. Ferrone, A. Massini *An O($log_2 N$) depth asymptotically nonblocking self-routing permutation network* IEEE Trans. on Comp., vol. 44, 1047-1050, 1995

R20 A. Clementi, G. A. De Biase, A. Massini *Fast parallel arithmetic on cellular automata* Complex Systems, vol. 8, 435-441, 1994

R21 G. A. De Biase, A. Massini *High efficiency redundant binary number representations for parallel arithmetic on optical computers* Optics & Laser Technology - Special Issue on Optical Computing, vol.26, n. 4, 219-224, 1994

R22 G. A. De Biase, A. Massini *Redundant Binary Number Representation for an Inherently Parallel Arithmetic on Optical Computers* Applied Optics, vol. 32, 659-664, 1993

R23 G. A. De Biase, A. Massini *Parallel Optical Arithmetic on Images by a Redundant Binary Number Representation* Applied Optics, vol. 29, 1587-1589, 1990

International conferences

C1 V. Arrigoni, A. Massini *Hybrid Solver for Quasi Block Diagonal Linear Systems*, Proc. PPAM, Bialystok, Poland, 2019, to appear LNCS 12043

C2 A. Calabrese, T. Mancini, A. Massini, S. Sinisi, E. Tronci *Generating T1DM Virtual Patients for In Silico Clinical Trials via AI-Guided Statistical Model Checking*, Proc. RCRA/RiCeRcA@AI*IA, Rende, Italy, 2019

C3 T. Mancini, F. Mari, A. Massini, I. Melatti, I. Salvo, S. Sinisi, E. Tronci, R. Ehrig, S. Röblitz, B. Leeners *Computing Personalised Treatments through In Silico Clinical Trials*, Proc. RCRA@FLoC, Oxford, United Kingdom, 2018

C4 T. Mancini, E. Tronci, I. Salvo, F. Mari, A. Massini, I. Melatti *Computing Biological Model Parameters by Parallel Statistical Model Checking*, Proc. IWBBIO (2), 542-554, Granada, Spain, 2015

C5 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *SyLVaaS: System Level Formal Verification as a Service* Proc. PDP, 476-483, Turku, Finland, 2015

C6 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *Simulator Semantics for System Level Formal Verification* Proc. Gandalf, 86-99, Genoa, Italy, 2015

C7 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *Anytime System Level Verification via Random Exhaustive Hardware In The Loop Simulation* Proc. 17th Euromicro Conf. on Digital Systems Design (DSD 2014) Verona, Italy, 2014

C8 T. Mancini, I. Salvo, F. Mari, I. Melatti, A. Massini, S. Sinisi, E. Tronci, F. Daví, T. Dierkes, R. Ehrig et al. *Patient-Specific Models from Inter-Patient Biological Models and Clinical Records* Formal Methods in Computer-Aided Design (FMCAD), Lausanne, Switzerland, 2014

C9 T. Mancini, F. Mari, A. Massini, I. Melatti, E. Tronci *System Level Formal Verification via Distributed Multi-Core Hardware in the Loop Simulation* Proc. 22nd Euromicro Int. Conf. on Parallel, Distributed and Network-Based Computing (PDP 2014) Turin, Italy, 2014

C10 T. Mancini, F. Mari, A. Massini, I. Melatti, F. Merli, E. Tronci *System Level Formal Verification via Model Checking Driven Simulation* Proc. CAV 2013 - 25th Int. Conf. on Computer Aided Verification, Saint Petersburg, Russia , 2013

C11 F. Alessi, A. Massini, R. Basili High Performance *Parallelization of COMPSYN on a Cluster of Multicore Processors with GPUs* Proc. 2nd Int. Workshop on Advances in High-Performance Computational Earth Sciences: Applications and Frameworks (IHPCES), Int. Con. on Computational Science, Omaha, Nebraska, USA, 2012

C12 F. Alessi, A. Massini, R. Basili *Accelerating the Production of Synthetic Seismograms by a Multicore Processor Cluster with Multiple GPUs* Proc. 20th Euromicro Int. Conf. on Parallel, Distributed and Network-Based Computing (PDP 2012) Garching, Germany, 2012

C13 N. Bartolini, T. Calamoneri, A. Massini, S. Silvestri *Variable density deployment and topology control for the solution of the sink-hole problem* Proc. ICST QShine 2009, Las Palmas de Gran Canaria, Spain, 2009

C14 N. Bartolini, A. Massini, S. Silvestri *P&P protocol: local coordination of mobile sensors for self-deployment* Proc. ACM Int. Conf. on Modeling, Analysis and Simulation of Wireless and Mobile Systems (ACM MSWIM 2009), Tenerife, Canary Island, Spain, 2009

C15 N. Bartolini, T. Calamoneri, T. La Porta, A. Massini, S. Silvestri *Autonomous deployment of heterogeneous mobile sensors* Proc. IEEE International Conference on Network Protocols (IEEE ICNP 2009), Princeton, New Jersey, USA, 2009 **Best Paper Award winner**

C16 A. Massini, M. T. Raffa *Using the LCP based Decomposition for Permutation Routing on (2 log N -1) Stage Interconnection Networks* Proc. International Conference on Parallel and Distributed Computing and Networks (PDCN2009), Innsbruck, Austria, 2009

C17 N. Bartolini, T. Calamoneri, E.G. Fusco, A. Massini, S. Silvestri *Autonomous deployment of self-organizing mobile sensors for a complete coverage* Proc. 3rd International Workshop on Self-Organizing Systems (IWSOS 2008), Vienna, Austria, 2008

C18 N. Bartolini, T. Calamoneri, E. G. Fusco, A. Massini, S. Silvestri *Snap and Spread: a self-deployment algorithm for mobile sensor networks* Proc. 4th IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS '08), Santorini, Greece, 2008

C19 T. Calamoneri, A. Massini, L. Torok, I. Vrto *Antibandwidth of complete k-ary tree* Proc. of 5th Cracow Conference on Graph Theory, Polland, Electronic Notes in Discrete Mathematics, 24, pp. 259-266, 2006

C20 T. Calamoneri, A. Massini *Nearly optimal three-dimensional layout of hypercube networks* Proc. of Graph Drawing 03, Italy, Lecture Notes in Computer Science, vol. 2912, 64-75, 2003

C21 G. A. De Biase, A. Massini *Parallel Sorting of n-strings in Kn Time* Proc. International Conference on Communications in Computing - CIC'2002, Las Vegas, Nevada, USA, 24-27, 2002

C22 T. Calamoneri, A. Massini A New Approach to the *Rearrangeability of (2 log N -1) Stage MINs* Proc. International Conference on Applied Informatics (AI2001), Austria, 2001

C23 A. Massini *All-to-all personalized communication on multistage interconnection networks* International Conference on Communications in Computing - CIC'2000, Las Vegas, Nevada, USA, 217-223, 2000

C24 T. Calamoneri, A. Massini *Efficiently checking the equivalence of multistage interconnection networks* Proc. 11th International Conference on Parallel and Distributed Computing Systems (PDCS'99), Cambridge, Massachusset, USA, 23-30, 1999

C25 A. Clementi, G. A. De Biase, A. Massini *Pipelined addition, accumulation and multiplication of binary numbers on cellular automata* Proc. Fourth Joint Conference on Information Science (JCIS'98), RTP, North Carolina, USA, 134-141, 1998

C26 G. Bongiovanni, G.A. De Biase, A. Massini, A. Monti *The shuffled mesh: a flexible and efficient model for parallel computing* Proc. 6th International Conference on Telecommunication Systems, Nashville, USA, 652-654, 1998

C27 T. Calamoneri, A. Massini *On three-dimensional layout of interconnection networks* Proc. of Graph Drawing 97, Roma, Italy, 64-75, 1997

C28 G. A. De Biase, A. Massini *Parallel Arithmetic on Optical Computers by Redundant Binary Number Representation* Proc. of International Conference on Application of Photonic Technology, Plenum Press, Toronto, Canada, 101-108, 1995

C29 G. A. De Biase, C. Ferrone, A. Massini *A quasi-nonblocking self-routing network which routes packets in log_2N time* Proc. of IEEE INFOCOM'93, S. Francisco, California, USA, 1375-1381, 1993