Advanced Architecture

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PART A

Student's Name

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***Matricola* number**

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Exercise 1 (6 points)	
Exercise 2 (6 points)	
Exercise 3 (5 points)	
Exercise 4 (3 points)	
Exercise 5 (6 points)	
Exercise 6 (6 points)	
Total (32 points)	

Exercise 1 (6 points) – Number representation

a) Determine the value of *n* for a residue number system with a three module set based on powers of 2 defined as $S=\{2^{n+1}+1; 2^{n+1}-1; 2^{n}\}$, such that the natural number range [0, 16299] is representable.

b) Represent A = 98 and B = 26 using S. Then compute the product P = A x B using the residue number representation, and verify the correctness of the representation of the result P.

c) Represent P in the **mixed radix representation** associated with S.

Exercise 2 (6 points) – Number representation

a) Represent X = –65 using the **RB (Redundant Binary)** representation.

b) Then represent X using a **redundant representation** with radix r=7 and the digit set [–5, 5] using 3 digits, providing different valid representations. Also specify how many values can be represented, the redundancy index, and the redundancy percentage.

Exercise 3 (5 points) – Circuit area and time

a) Consider the moduli set T= {7, 11, 13, 16} for a residue number system. Specify which ripple-carry adder modules should be used to design an adder for numbers represented using T, assuming radix-2 representation for each module and neglecting the logic required to ensure that the result lies within the correct range. Then compute the circuit area and the time required to perform 200 additions.

b) Now consider a pipelined adder sized to operate over the range defined by the moduli set T in point a). Compute the area of the circuit and the time required to perform 200 additions.

c) Determine the number of additions for which the pipelined adder becomes more convenient, if any.

Exercise 4 (3 points) Gustafson-Barsis' law

a) Briefly explain the difference between the Gustafson-Barsis' law and the Amdahl's law.

b) The analysis of a program has shown a speedup of 8.5 when running on 24 cores. What is the serial fraction according to Gustafson-Barsis' law? And according to Amdahl's law?

c) Considering the serial fraction obtained in point b), compute the speedup when using 32 cores according to Gustafson-Barsis' law and Amdahl's law.

Exercises 5 (6 points) Amdhal law

The following measurements are recorded for different instruction classes in an instruction set running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles Per Instruction
Arithmetic and logic	10	6.8
Load and store	14	4.2
Branch	8	7.6
Others	12	5.0

Assume that "*Load and store*" instructions can be improved, achieving a speedup factor of 9, and that "*Branch*" instructions can be improved, achieving a speedup of 15.

a) Compute the **speedup** obtained by introducing only one enhancement and both enhancements, using **Amdahl's law**, and identify which alternative is more cost-effective.

b) Then compute the new CPI (Cycle Per Instruction) value for the two cases, using the specified speedup.

Exercises 6 (6 points) Performance equation

Suppose we have the following measurements, where we consider the set of Arithmetic and Logic instructions (A&L), the **subset** of Arithmetic instructions (AR) and the **subset** of integer Multiplications and Divisions (MD):

Frequency of A&L operations = 40%
Average CPI of A&L operations = 6
Frequency of AR = 20%
CPI of AR = 4.5
Frequency of MD = 10%
CPI of MD = 8
Average CPI of other (than A&L) instructions = 3.5

Assume that you have the following design alternatives: i) reduce the average CPI of A&L instructions to 5; ii) reduce the CPI of AR operations to 3.4; iii) reduce the average CPI of MD operations to 6.4.
Compare these three design alternatives using the **processor performance equation** and compute the speedup in each case.