Advanced Architecture

Prof. A. Massini

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PART B

Student's Name

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***Matricola* number**

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Exercise 1 (5 points)	
Exercise 2 (5 points)	
Exercise 3 (6 points)	
Exercise 4 (5 points)	
Exercise 5 (6 points)	
Exercise 6 (5 points)	
Total (32 points)	

Exercise 1 (5 points) – Interconnection Networks

Briefly explain how the routing algorithm works for a **Benes network.**

Consider a Benes network of size N=8 and show how to realize permutation $P = \begin{pmatrix} 0\,1\,2\,3\,4\,5\,6\,7 \\ 6\,0\,2\,7\,5\,4\,1\,3 \end{pmatrix}$

Exercise 2 (5 points) – Interconnection networks

Illustrate the design of an XGFT(4; 2, 1, 4, 2; 1, 4, 1, 2), specifying how many nodes there are on each level, how many parents and children they have, and then showing the drawing of the network(remember the recursive construction).

Exercise 3 (6 points) – Interconnection Networks

a) Design a Clos network of size 475 x 475, having **only square crossbar modules of size 16**, composing them as necessary, depending on the stage considered. Specify the size and number of switches for each stage. Consider both cases, **strictly non-blocking** and **rearrangeable** networks.

b) Discuss what network is more advantageous, after calculating:
   i. the cost of the crossbar 475 x 475
   ii. the cost of the Clos networks strictly non-blocking and rearrangeable non-blocking designed in the previous point
   iii. the cost of the Benes with 512 inputs/outputs

Exercise 4 (5 points) – Quantum circuits

a) Compute the state vector of a two-qubit system composed by the two qubits:

$$\psi_1 = \frac{1}{3}\,|0\rangle + \frac{2\sqrt{2}}{3} i|1\rangle$$

$$\psi_3 = \frac{\sqrt{3}}{2}\,|0\rangle - \frac{1}{2} i|1\rangle$$

b) Verify the normalization condition of the two-qubit system.

c) Compute the probability of measuring $|00\rangle$ and the probability of measuring $|10\rangle$.

Exercise 5 (6 points) – Quantum circuits

a) Consider gate associated to the matrix $V = \frac{1}{2}\begin{bmatrix} 1+i & 1-i \\ 1-i & 1+i \end{bmatrix}$ and show the matrix of $U = V \otimes Z$ where $\mathrm{Z} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$ and show that U is unitary.

b) Consider the circuit composed by the gate represented by gate U above followed by a CNOT. Show how the circuit acts on the statevector $[\ \frac{i}{4};\ \frac{\sqrt{3}}{2\sqrt{2}};\ \frac{1}{4};\ \frac{\sqrt{2}}{2}\ i]$.

Exercise 6 (5 points) - GPU & CUDA

Technical specifications	Compute capability (version)									
	1.0	**1.1**	**1.2**	**1.3**	**2.x**	**3.0**	**3.5**	**3.7**	**5.0**	**5.2**
Maximum dimensionality of grid of thread blocks	2				3					
Maximum x-dimension of a grid of thread blocks	65535					2^{31}-1				
Maximum y-, or z-dimension of a grid of thread blocks	65535									
Maximum dimensionality of thread block	3									
Maximum x- or y-dimension of a block	512				1024					
Maximum z-dimension of a block	64									
Maximum number of threads per block	512				1024					
Warp size	32									
Maximum number of resident blocks per multiprocessor	8					16			32	
Maximum number of resident warps per multiprocessor	24		32		48	64				
Maximum number of resident threads per multiprocessor	768		1024		1536	2048				
Technical specifications	**1.0**	**1.1**	**1.2**	**1.3**	**2.x**	**3.0**	**3.5**	**3.7**	**5.0**	**5.2**
	Compute capability (version)									

Consider a matrix of size 4850x2200. You would like to assign one thread to each matrix element.

a) How would you select the **2D grid** dimensions and **2D block** dimensions of your kernel to **minimize the number of idle threads** on a device having compute capability 3.7? Specify how many idle threads you have.

b) Repeat considering a device with compute capability 2.x