

Intensive Computation

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Part B

Student's Name

Matricola number

Exercise 1 (4 points)	
Exercise 2 (4 points)	
Exercise 3 (4 points)	
Question 1 (3 points)	
Question 2 (3 points)	
Exercise 4 (4 points)	
Exercise 5 (3 points)	
Exercise 6 (3 points)	
Exercise 7 (4 points)	
Total (32 points)	

Exercise 1 (4 points) - GPU & CUDA

You need to write a kernel that operates on a matrix of size **680x800**. You would like to assign one thread to each matrix element. You would like your thread blocks to use the maximum number of threads per block possible on your device, having compute capability 3.5.

- How would you select the dimensions of a **2D grid** and **2D blocks** for your kernel? Consider the two cases of **rectangular** and **square blocks** for the x and y dimensions.
- What is the best choice for grid and block dimensions with respect to the number of idle threads?

[illegible]

Exercise 2 (4 points) – Interconnection Networks – CLOS

Design a Clos network of size 100 x 100, using modules 8x8. In the first stage, only 8 inputs per module are allowed.

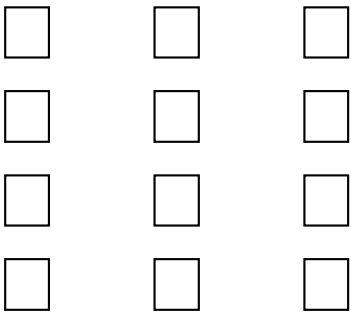
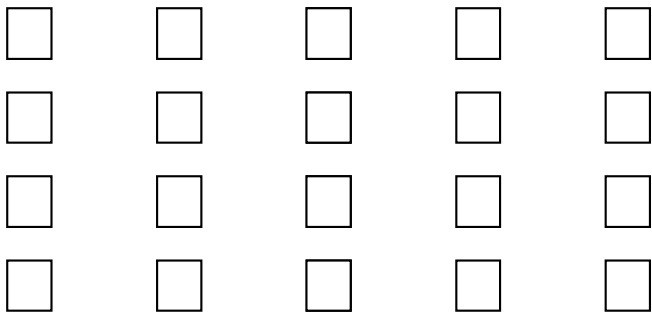
Consider both cases, strictly non-blocking and rearrangeable network.

Compare the cost of the crossbar 100 x 100 and the Clos network, strictly non-blocking and rearrangeable, designed in the previous point, giving the gain in both cases.

Exercise 3 (4 points) – Interconnection networks – (2 log N - 1) MIN

Briefly explain how the looping algorithm works.

Complete the scheme of the Benes (left) and Butterfly (right) networks. Show the switch setting to realize permutation $P = \begin{pmatrix} 01 & 23 & 45 & 67 \\ 15 & 06 & 47 & 23 \end{pmatrix}$ according to the looping algorithm for the Benes network and the self-routing algorithm for the Butterfly.



Question 1 (3 points)

Briefly explain the performance equation

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Question 2 (3 points)

Briefly describe the Hypercube, mesh and tree networks, highlighting their differences.

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Exercises 4 (4 points) Amdhal Law

The following measurements are recorded with respect to the different instruction classes for the instruction set running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Arithmetic and logic	5	8
Load and store	6	3
Branch	6	5
Others	8	4

Assume that “*Arithmetic and logic*” instructions can be modified so that they take 5 cycle per instruction instead of 8 as in the table. Compute the speedup obtained by introducing this enhancement using the **Amdhal law**.

How many cycles should “*Branch*” instructions consist of to reach at least the same speedup obtained modifying the number of cycles of “*Arithmetic and logic*” instructions as above?

Exercise 5 (3 points) – Number representation

Given the values $A = 11\ 00\ 00\ 10\ 11$ and $B = 00\ 10\ 00\ 00\ 11$ in the RB representation, convert them in decimal.

Show the execution of operation $A+B$. Verify the value of the results.

Exercise 6 (3 points) - Number representation

- Determine two ways to choose the moduli set for using the **residue number system** to represent values in the number range $[0; 359]$, considering a moduli set consisting of **3 moduli** and a moduli set consisting of **4 moduli**.
- Compare the two different choices with respect to the number of bits necessary for the representation, and consider also the number of bits needed for representing the range $[0; 359]$ with the conventional binary system.

Represent $A = 43$ and $B = 66$ using the considered different choices of the moduli sets, and show how to compute the sum $A + B$.

Exercise 7 (4 points) – Arithmetic circuit time and area

Explain the difference between a pipelined multiplier for **unsigned** and **signed binary values** and compare the **area** required by the two **multipliers**.