

# Intensive Computation

Prof. A. Massini

24 July 2018

## Part B

- Student's Name -

---

- *Matricola* number -

---

Exercise 1 (4 points)	
Exercise 2 (4 points)	
Exercise 3 (4 points)	
Exercise 4 (4 points)	
Exercise 5 (4 points)	
Exercise 6 (4 points)	
Exercise 7 (3 points)	
Question 1 (3 points)	
Question 2 (3 points)	
Total (33 points)	

**Exercise 1 (4 points) – Interconnection Networks**

- a) Design a Clos network of size  $325 \times 325$ , using in the first stage modules having 36 inputs. Consider both cases, **strictly non-blocking** and **rearrangeable** network.
- b) Compare the cost of the crossbar  $325 \times 325$  and the Clos network, strictly non-blocking and rearrangeable, designed in the previous point.

## Exercise 2 (4 points) - GPU & CUDA

You need to write a kernel that operates on a 3D matrix of size **300x300x300**. You would like to assign one thread to each matrix element. You would like your thread blocks to use the **maximum number of threads per block** possible on your device, having compute capability 3.5.

How would you select the dimensions of **grid** and **blocks** for your kernel so as to minimize the number of idle threads?

Technical specifications	Compute capability (version)									
	1.0	1.1	1.2	1.3	2.x	3.0	3.5	3.7	5.0	5.2
Maximum dimensionality of grid of thread blocks	2				3					
Maximum x-dimension of a grid of thread blocks	65535					2 <sup>31</sup> -1				
Maximum y-, or z-dimension of a grid of thread blocks	65535									
Maximum dimensionality of thread block	3									
Maximum x- or y-dimension of a block	512					1024				
Maximum z-dimension of a block	64									
Maximum number of threads per block	512					1024				
Warp size	32									
Maximum number of resident blocks per multiprocessor	8					16			32	
Maximum number of resident warps per multiprocessor	24		32		48	64				
Maximum number of resident threads per multiprocessor	768		1024		1536	2048				
Technical specifications	1.0	1.1	1.2	1.3	2.x	3.0	3.5	3.7	5.0	5.2
	Compute capability (version)									

### Exercises 3 (4 points) Amdhal Law

The following measurements are recorded with respect to the different instruction classes for the instruction set running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Arithmetic and logic	8	6
Load and store	5	4
Branch	6	5
Others	5	4

Assume that "*Load and store*" instructions can be modified so that they take 2 cycles per instruction instead of 4, and "*Arithmetic and logic*" instructions can be modified so that they take 4 cycle per instruction instead of 6 as in the table. Compute the speedup obtained by introducing **only one** enhancement and **both** enhancements using the **Amdhal law**.

#### Exercises 4 (4 points) Performance equation

Suppose we have made the following measurements, where we are considering Arithmetic and FP (Floating Point) instructions:

Frequency of Arithmetic operations = 45%

Average CPI of Arithmetic operations = 4.5

Average CPI of other instructions = 3.0

Frequency of FP operations = 10%

CPI of FP = 6.0

Note that Arithmetic operations include Floating point operations.

Assume that the two design alternatives are to decrease the CPI of FP to 4.0 or to decrease the average CPI of Arithmetic operations to 3.5.

Compare these two design alternatives using the processor **performance equation**, and compute the speedup in **both cases**.

**Exercise 5 (4 points) – Number representation**

Given the values  $A = 00\ 01\ 00\ 01\ 10$  and  $B = 00\ 00\ 11\ 01\ 11$  in the RB (Redundant Binary) representation, show the execution of operation  $A - B$ .

**Exercise 6 (4 points) - Number representation**

- Represent the natural number range  $[0; 190]$  using the **residue number system**, considering **two** different choices of the moduli set, consisting of **3 moduli**.
- Represent  $A = 48$  and  $B = 35$  using the considered different choices of the moduli sets and show how to compute the sum  $A + B$ .



