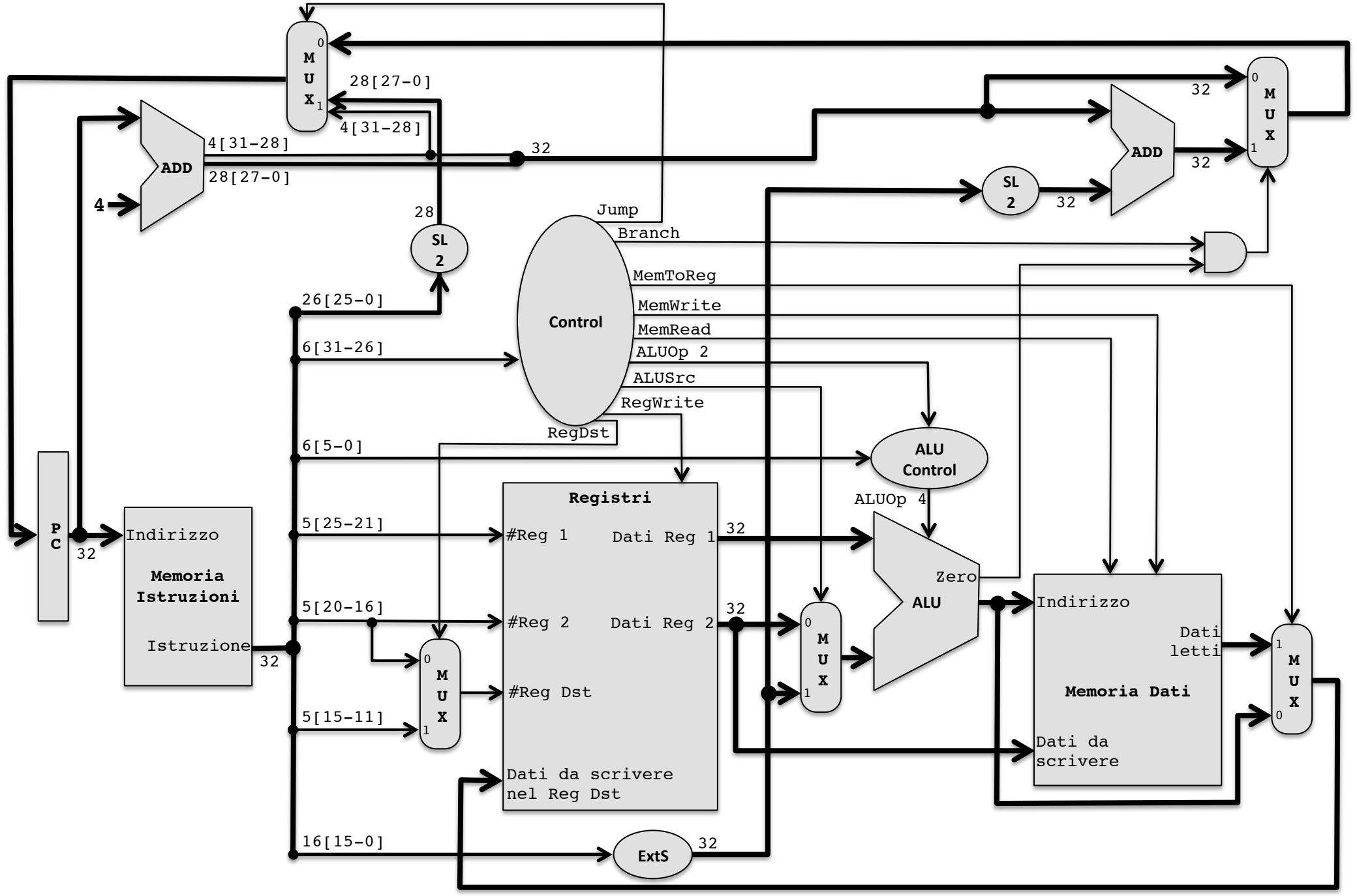
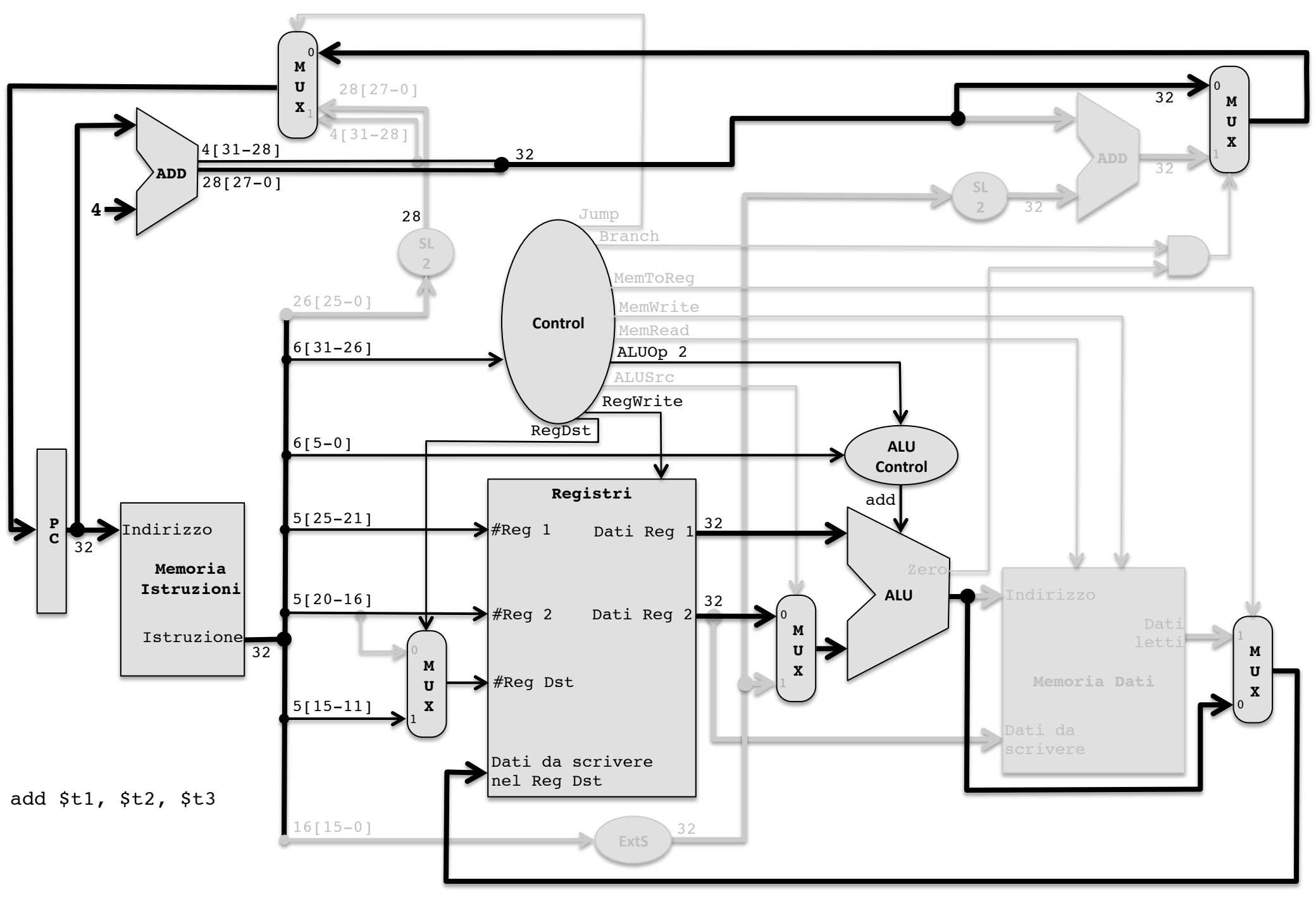
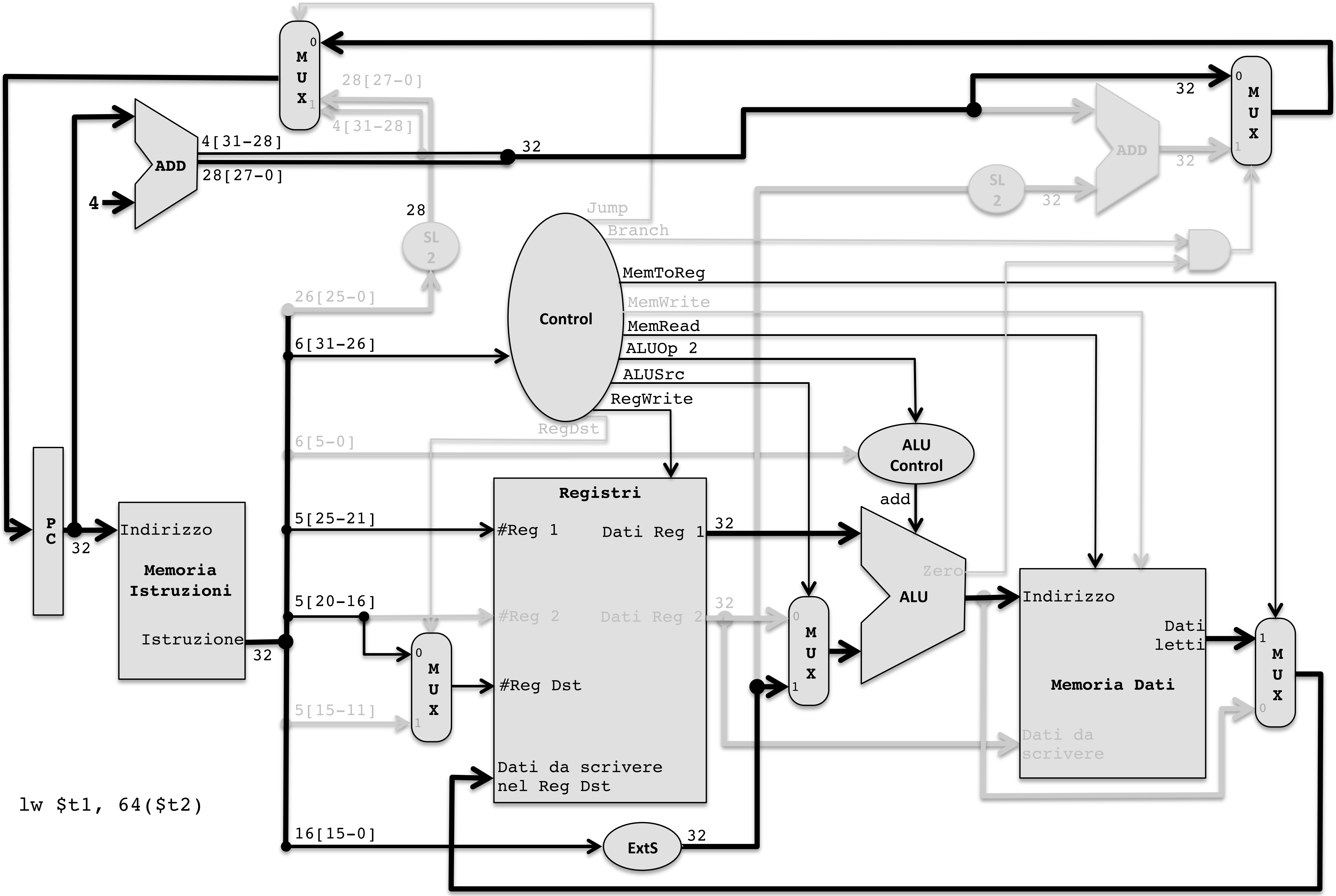
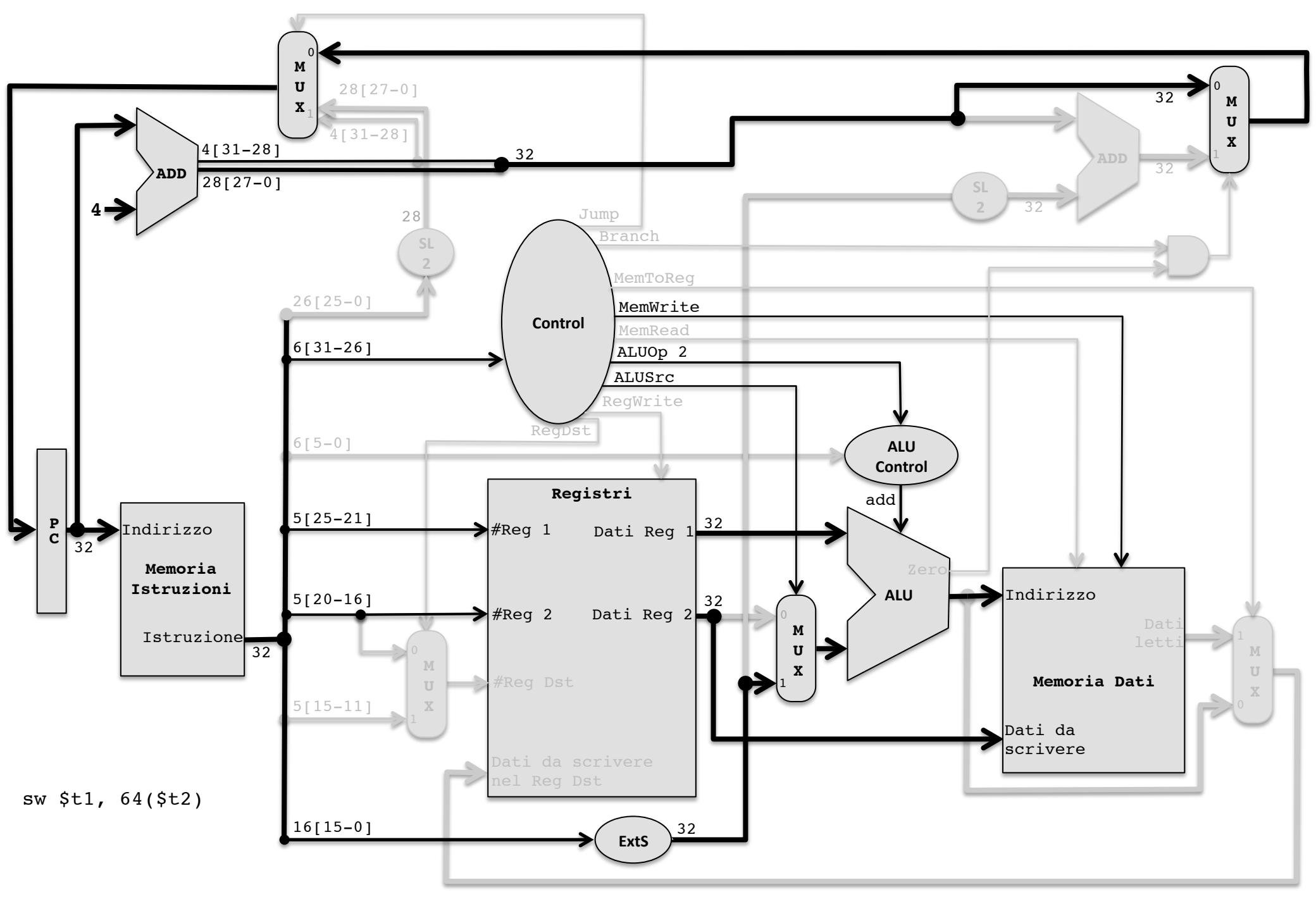
Implementazione ad un ciclo di clock di MIPS (solamente le istruzioni: `add`, `sub`, `and`, `or`, `xor`, `slt`, `lw`, `sw`, `beq`, `j`)

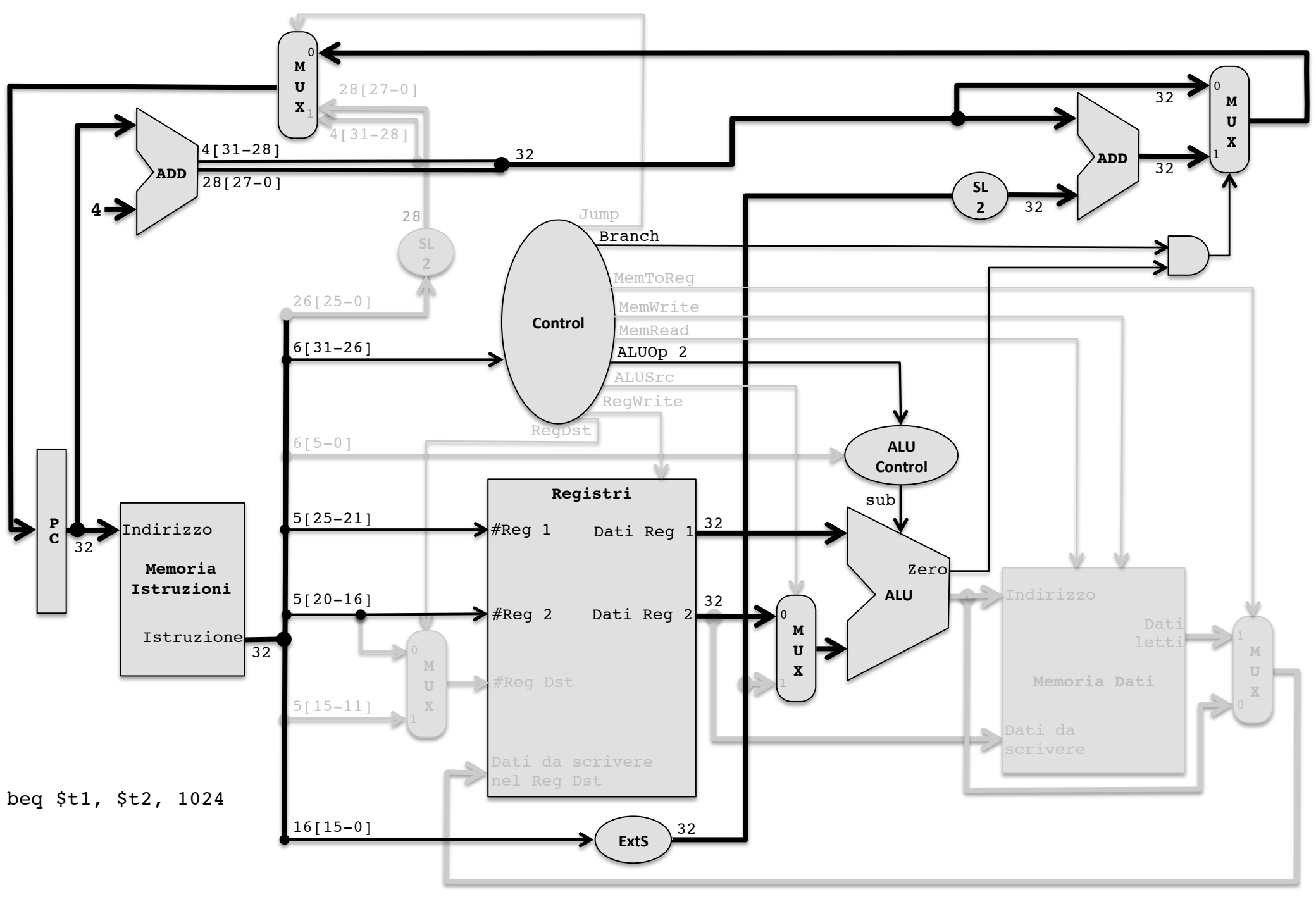


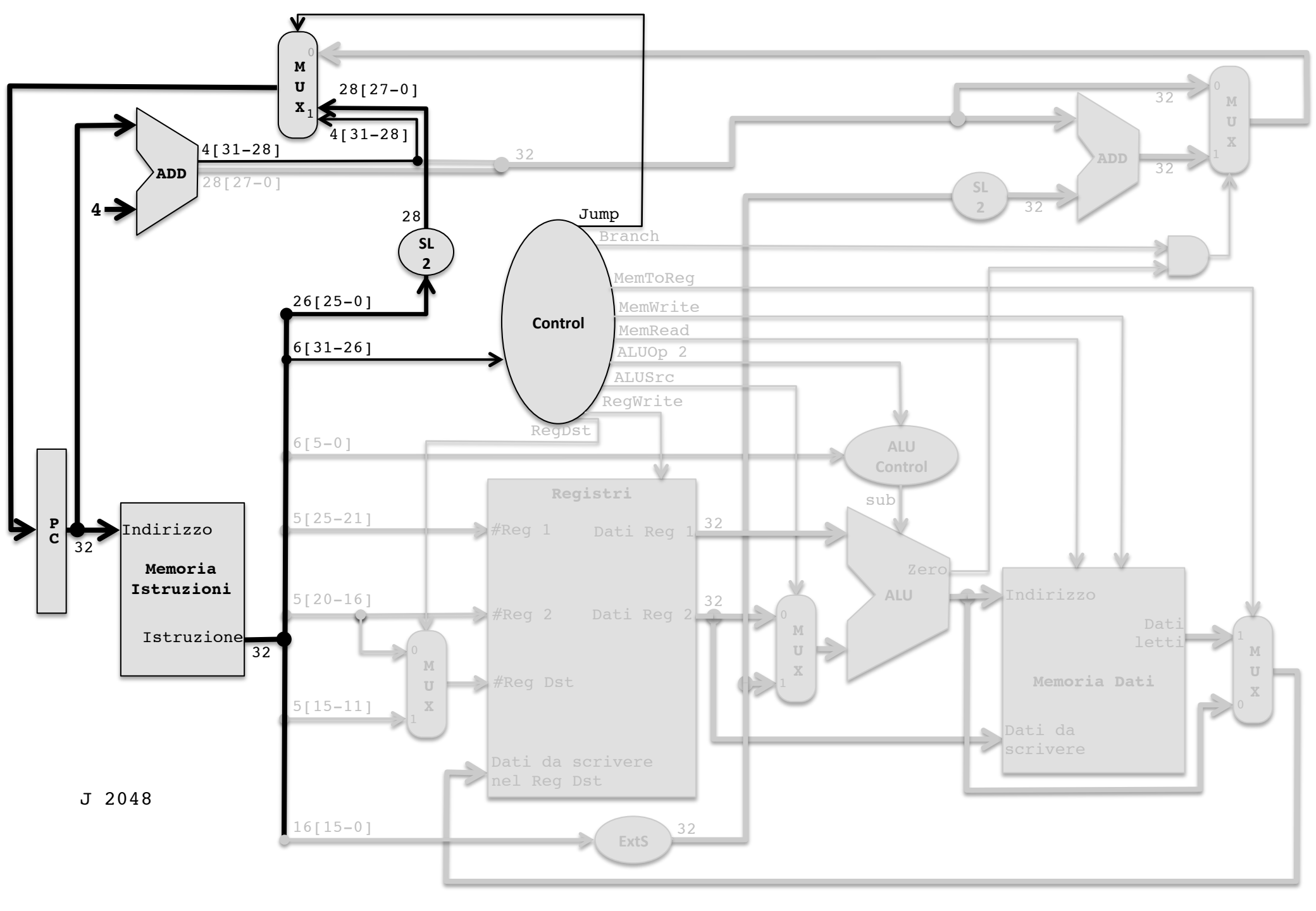

MUX
0
1
28[27-0]
4[31-28]
ADD
4[31-28]
28[27-0]
4
32
28
SL 2
Jump
Branch
MemToReg
MemWrite
MemRead
ALUOp 2
ALUSrc
RegWrite
RegDst
Control
26[25-0]
6[31-26]
6[5-0]
5[25-21]
5[20-16]
5[15-11]
16[15-0]
ExtS
32
ADD
SL 2
32
32
MUX
0
1
PC
32
Indirizzo
Memoria Istruzioni
Istruzione
32
Registri
#Reg 1
Dati Reg 1
#Reg 2
Dati Reg 2
#Reg Dst
Dati da scrivere nel Reg Dst
32
32
MUX
0
1
ALU Control
add
ALU
Zero
Indirizzo
Memoria Dati
Dati letti
Dati da scrivere
MUX
1
0
add $t1, $t2, $t3



M U X
0
1
28[27-0]
4[31-28]
ADD
4[31-28]
28[27-0]
32
4
28
SL 2
Jump
Branch
Control
MemToReg
MemWrite
MemRead
ALUOp 2
ALUSrc
RegWrite
RegDst
26[25-0]
6[31-26]
6[5-0]
5[25-21]
5[20-16]
5[15-11]
16[15-0]
P C
32
Indirizzo
Memoria Istruzioni
Istruzione
32
Registri
#Reg 1
Dati Reg 1
#Reg 2
Dati Reg 2
#Reg Dst
Dati da scrivere nel Reg Dst
32
32
ALU Control
add
ALU
Zero
ExtS
32
Indirizzo
Dati letti
Memoria Dati
Dati da scrivere
ADD
SL 2
32
32
32
lw $t1, 64($t2)


M U X
0
1
28[27-0]
4[31-28]
ADD
4[31-28]
28[27-0]
4
32
28
SL 2
Jump
Branch
MemToReg
MemWrite
MemRead
ALUOp 2
ALUSrc
RegWrite
RegDst
Control
26[25-0]
6[31-26]
6[5-0]
ALU Control
add
PC
32
Indirizzo
Memoria Istruzioni
Istruzione
32
Registri
5[25-21]
#Reg 1
Dati Reg 1
32
5[20-16]
#Reg 2
Dati Reg 2
32
5[15-11]
#Reg Dst
Dati da scrivere nel Reg Dst
ALU
Zero
Indirizzo
Dati letti
Memoria Dati
Dati da scrivere
16[15-0]
ExtS
32
sw $t1, 64($t2)


M U X
0
1
28[27-0]
4[31-28]
ADD
4[31-28]
28[27-0]
4
32
32
ADD
32
M U X
SL 2
32
28
SL 2
Jump
Branch
MemToReg
MemWrite
MemRead
ALUOp 2
ALUSrc
RegWrite
RegDst
Control
26[25-0]
6[31-26]
6[5-0]
ALU Control
sub
PC
32
Indirizzo
Memoria Istruzioni
Istruzione
32
Registri
#Reg 1
Dati Reg 1
32
5[25-21]
5[20-16]
#Reg 2
Dati Reg 2
32
Zero
ALU
Indirizzo
Dati letti
Memoria Dati
Dati da scrivere
M U X
#Reg Dst
5[15-11]
Dati da scrivere nel Reg Dst
16[15-0]
ExtS
32
beq $t1, $t2, 1024


M
U
X
0
1
28[27-0]
4[31-28]
ADD
4[31-28]
28[27-0]
4
32
28
SL
2
Jump
Branch
MemToReg
MemWrite
MemRead
ALUOp 2
ALUSrc
RegWrite
RegDst
Control
26[25-0]
6[31-26]
6[5-0]
5[25-21]
5[20-16]
5[15-11]
16[15-0]
PC
32
Indirizzo
Memoria
Istruzioni
Istruzione
32
Registri
#Reg 1
Dati Reg 1
#Reg 2
Dati Reg 2
#Reg Dst
Dati da scrivere
nel Reg Dst
32
32
32
ALU
Control
sub
ALU
Zero
Indirizzo
Memoria Dati
Dati
letti
Dati da
scrivere
ExtS
32
J 2048