

# Exam of Computer Architectures – UNIT 1 - September 13th, 2021

Surname \_\_\_\_\_ Name \_\_\_\_\_ Matr.Numb. \_\_\_\_\_

**Exercise 1 (3 points):** Turn into base 5, by showing all steps, the following number in base 10: 120,15.

120	5
24	0
4	4
0	4

$0,15 \times 5 = 0,75$
$0,75 \times 5 = 3,75$
$0,75 \times 5 = 3,75$
⋮

$\Rightarrow 440,0\overline{3}$

**Exercise 2 (3 points):** Sum the following numbers in IEEE half-precision format:  
 $\langle 0; 01010; 1110000000 \rangle$  and  $\langle 1; 10000; 1100000000 \rangle$

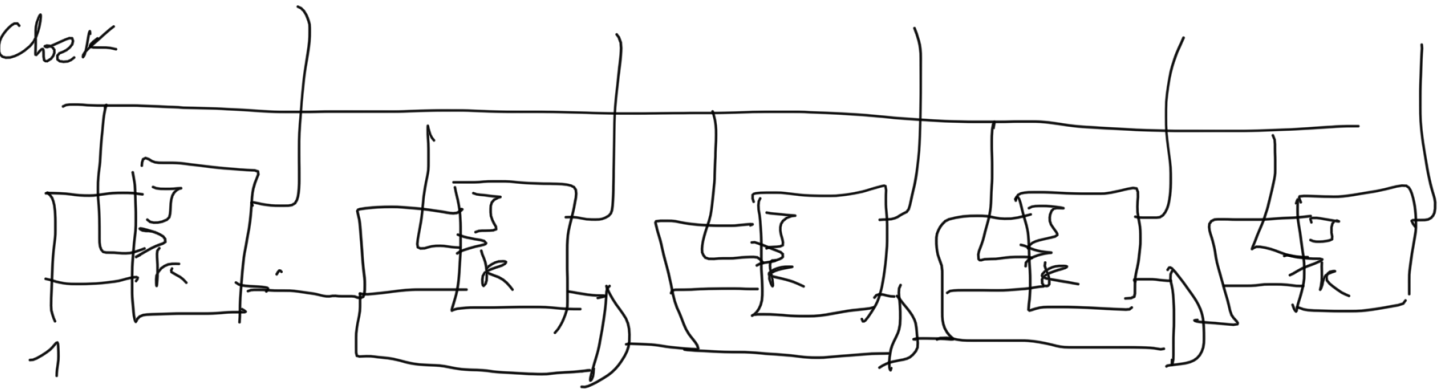
↓

$\langle 0; 00000; 000001110 \rangle$

1,	<sup>0</sup>	<sup>1</sup>	<sup>1</sup>	<sup>1</sup>	<sup>1</sup>	<sup>1</sup>	<sup>2</sup>	-
1,	<del>1</del>	<del>0</del>	<del>0</del>	<del>0</del>	<del>0</del>	<del>0</del>	<del>0</del>	-
0,	0	0	0	0	1	1	1	0
1,1011100010								

$\langle 1; 10000; 1011100010 \rangle$

**Exercise 3 (2 points):** Draw the circuit schema of a downwards synchronous counter modulo 32.



**Exercise 4 (2+2+2+1 points):**

a) Write the truth table of the function that, taken a 3 bits integer (in 2-complement), returns its double represented as a 4 bits integer (in 2-complement). Assume that 100 will never be received.

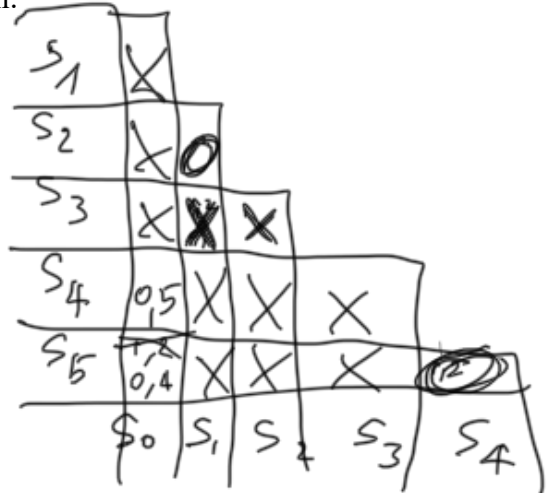
b) Implement the most signifying bit of the obtained function with a MUX 2-to-1:

c) Write the minimal POS formulae associated to the two less signifying bits of the function:

d) Implement the whole function with a ROM:

**Exercise 5 (6 points):** Consider the following automaton:

	0	1
S0	S1/0	S0/0
S1	S2/0	S3/1
S2	S2/0	S3/1
S3	S1/0	S0/1
S4	S1/0	S5/0
S5	S2/0	S4/0



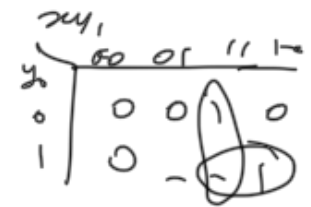
Minimize it and write down the associated sequential net that uses a JK FF for the most signifying bit and a T FF for the less signifying one.

MIN; AUT. :  $S_0 \equiv S_4 \neq S_5$   
 $S_1 \equiv S_2$

$S_{0,4,5} \Rightarrow Q_0 \rightarrow 00$   
 $S_{1,2} \Rightarrow Q_1 \rightarrow 01$   
 $S_3 \Rightarrow Q_2 \rightarrow 10$

	0	1
$Q_0$	$Q_1 / 0$	$Q_0 / 0$
$Q_1$	$Q_1 / 0$	$Q_2 / 1$
$Q_2$	$Q_1 / 0$	$Q_0 / 1$

$x \ y_1 \ y_0$	$Y_1 \ Y_0 \ z$	$J_1 \ K_1 \ T_0$
0 0 0	0 1 0	0 - 1
0 0 1	0 1 0	0 - 0
0 1 0	0 1 0	- 1 -
0 1 1	- - -	- - -
1 0 0	0 0 0	0 - 0
1 0 1	1 0 1	1 - 1
1 1 0	0 0 1	- 1 -
1 1 1	- - -	- - -



$Z = x y_1 + x y_0$   
 $= x (y_1 + y_0)$



$T_0 = \bar{x} \bar{y}_2 + x y_2$   
 $= x \otimes y_2$



$J_1 = x y_0$



$K_1 = 1$

**Exercise 6 (4 points):** Design an automaton that receives in input two bit sequences and gives in output 1 whenever the last three bits of the first sequence followed by the last two bits of the second sequence represent a natural number in base 2 that is a multiple of 8. The first two outputs are ignored, hence you can handle them in the way that makes the automaton simpler.

**Exercise 7 (5 points):** We have four source registers  $S_0$ ,  $S_1$ ,  $S_2$  and  $S_3$  and two destination registers  $D_0$  and  $D_1$ . Implement an interconnection such that:

- The index of the source register to be moved into  $D_0$  is given by calculating  $(S_0+2) \bmod 4$ ;
- $D_1$  receives the content of  $S_1$ , if  $S_0$  is greater than or equal to  $S_2$ ;  $S_3$  otherwise.

In both cases, transfers are enabled only if  $S_3$  is even.