## Exercises on the topics of class 14

## Exercises with solutions

Ex. 1. A 4 variables $\mathrm{BF} f\left(\mathrm{x}_{4}, \mathrm{x}_{3}, \mathrm{x}_{2}, \mathrm{x}_{1}\right)$ holds 1 if $\mathrm{x}_{4}+\mathrm{x}_{2} \mathrm{x}_{1}=0$, whereas it is not specified (don't care terms) if $\mathrm{x}_{4} \mathrm{x}_{1}=1$. Design a circuit that implements f through a PLA and a MUX.

SOLUTION:
The TT of the function is:

| $\mathbf{x} \mathbf{4}$ | $\mathbf{x} \mathbf{3}$ | $\mathbf{x} \mathbf{2}$ | $\mathbf{x} \mathbf{1}$ | $\mathbf{f}$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | - |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | - |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | - |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | - |

The KM is:

| x2 x1 <br> $\mathrm{x} 4 \times 3 \backslash$ |  |  |  | 00 |
| :--- | :---: | :---: | :---: | :---: |
| 00 | 1 | 1 | 0 | 1 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | x | x | 0 |
| 10 | 0 | x | x | 0 |

and so, the resulting minimal SOP for f is $\underline{\mathrm{X}}_{2} \mathrm{x}_{1}+\underline{\mathrm{x}}_{4} \underline{\mathrm{x}}_{1}$ From this, we can obtain the PLA:


For the realization with a MUX, we can choose a 16 -to-1. For the don't care symbols, we can indifferently choose to put a 0 or a 1 in that entrance (in this solution, we choose 0 for all don't cares):


Ex. 2. Design a combinatorial circuit that computes function $y=x+3$, where $x$ is a 4-bits 2 complement integer in $[-8,7]$ and $y$ is codified in the same format. Put "don't care" symbols whenever y cannot be represented in the given format.

Use a PLA for the two less signifying bits of y , a ROM for all the function and a MUX 8-to-1 for the second most signifying bit.

SOLUTION:
The required function is:

| $\boldsymbol{X}_{\mathbf{3}}$ | $\boldsymbol{X}_{\mathbf{2}}$ | $\boldsymbol{X}_{\boldsymbol{I}}$ | $\boldsymbol{X}_{\mathbf{0}}$ | $\boldsymbol{Y}_{\mathbf{3}}$ | $\boldsymbol{Y}_{\mathbf{2}}$ | $\boldsymbol{Y}_{\boldsymbol{I}}$ | $\boldsymbol{Y}_{\mathbf{0}}$ |
| :---: | :---: | :---: | :---: | ---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | - | - | - | - |
| 0 | 1 | 1 | 0 | - | - | - | - |
| 0 | 1 | 1 | 1 | - | - | - | - |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

We can now compute the minimal SOP for the two less signifying bits:


and so the PLA is:


The ROM is codified by looking at the TT of the function:


For the MUX, we use as control lines $X_{3}, X_{2}$ and $X_{1}$. Don't care symbols can be freely put to 0 or 1 , but in our case it turns out that all 1 s is a good option. So, the resulting circuit is:


## Exercises without solutions

Ex. 1. Design a PLA for the 4 -variables function $f(x 3, x 2, x 1, x 0)=m 2+m 3+m 4+m 9$ that is not defined (don't care) in m0, m1, m6 and m11.

Ex. 2. Design two 4-to-1 MUXs for the two 3 -variables BFs $f(a 2, a 1, a 0)=m 0+m 3+m 6+m 7$ and $g(a 2, a 1, a 0)=m 2+m 4+m 5+m 6$.

Ex. 3. Consider the following BF:

| $x$ | $y$ | $z$ | $t 1$ | $t 2$ | $t 3$ | $t 4$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

a) Design a ROM for this BF.
b) Compute $t 1$ and $t 4$ through a PLA.
c) Compute $t 2$ and $t 3$ through a 4-to-1 MUX and a 2-to-1 MUX, respectively.

