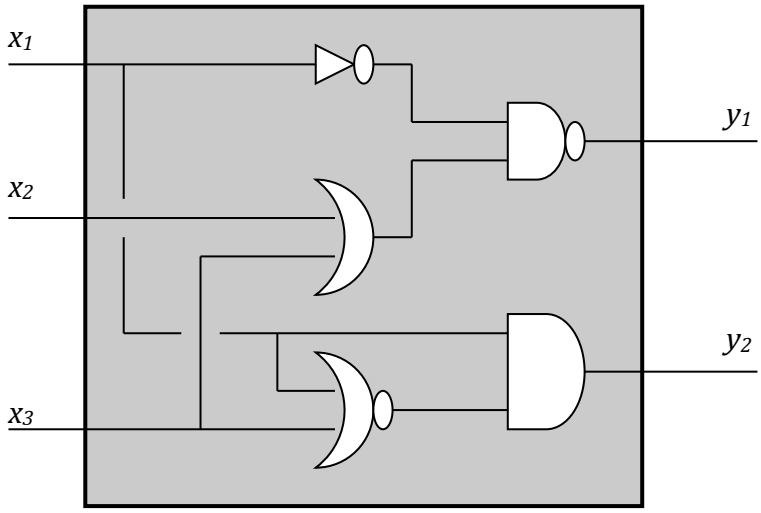
Exercises on the topics of class 12

Exercises with solutions

Ex. 1. Analyze the following circuit:

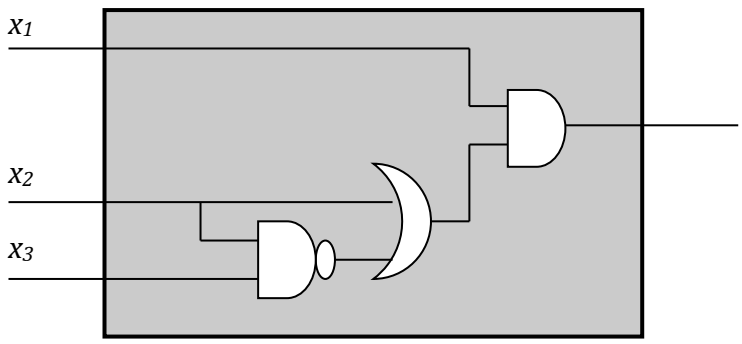


SOLUTION:

The circuit corresponds to the pair of BEs: $< \overline{x_1} \cdot (x_2 + x_3) \ , \ \overline{(x_3 + x_1) \cdot x_1} >$
Hence, it calculates the following binary BF:

x1	*x2*	*x3*	*f*
0	0	0	1 0
0	0	1	0 0
0	1	0	0 0
0	1	1	0 0
1	0	0	1 0
1	0	1	1 0
1	1	0	1 0
1	1	1	1 0

Ex. 2. Minimize the following circuit:

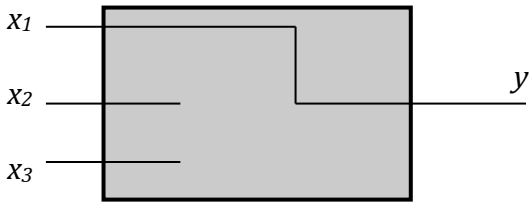


SOLUTION:

The given circuit corresponds to the BE:

$$(\overline{(x_2 \cdot x_3)} + x_2) \cdot x_1 = (\bar{x}_2 + \bar{x}_3 + x_2) \cdot x_1 = 1 \cdot x_1 = x_1$$

where we used De Morgan's law, the axiom of the complement, the annihilation law and the axiom for the neutral element. Hence, the given circuit corresponds to



Ex.3. Design the control circuit of a lift able to react to the following events

- Faulty door closure
- Abrupt stop at the floor
- Slow reaction to calling
- Sudden stop during the run

and that gives in output a warning signal every time that at least two of these events occur simultaneousy (in the same run of the lift).

SOLUTION:

Let's associate a boolean variable to every event:

- Faulty door closure → C
- Abrupt stop at the floor → A
- Slow reaction to calling → T
- Sudden stop during the run → F
- Warning signal → W

The computed BF is:

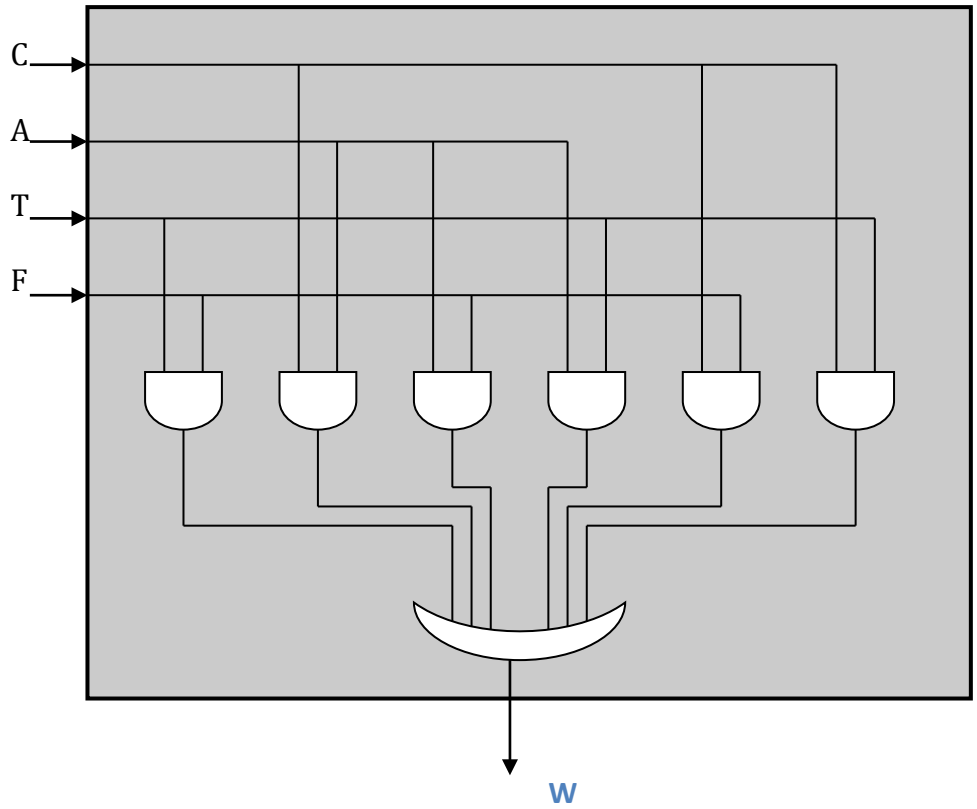
C	A	T	F	W
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

By using the KMs we obtain:

C A \ T F	0 0	0 1	1 1	1 0
0 0	0	0	1	0
0 1	0	1	1	1
1 1	1	1	1	1
1 0	0	1	1	1

and so $W = T \cdot F + C \cdot A + A \cdot F + A \cdot T + C \cdot F + C \cdot T$

Hence, the circuit is:



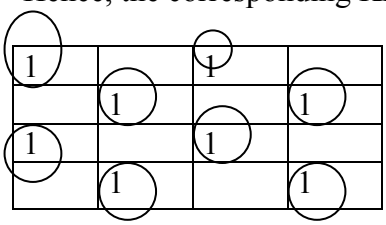
Ex. 4. Design a circuit with 7 bits in input X6X5…X0 and produces in output 8 bits: the 7 most signifying ones (Y7Y6..Y1) are equal to X6X5…X0, respectively, whereas Y0=1 if X3X2X1X0 contains an even number of 1s, Y0=0 othertwise.

SOLUTION:

Clearly, $Y_i=X_{i-1}$ for i = 1,…,7. For Y0, its truth table is:

X3	X2	X1	X0	Y0
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Hence, the corresponding KM is:



from which

$$Y0= \bar{X}_3\bar{X}_2\bar{X}_1\bar{X}_0 + \bar{X}_3\bar{X}_2X_1X_0 + \bar{X}_3X_2\bar{X}_1X_0 + \bar{X}_3X_2X_1\bar{X}_0 + X_3X_2\bar{X}_1\bar{X}_0 + X_3X_2X_1X_0 + X_3\bar{X}_2\bar{X}_1X_0 + X_3\bar{X}_2X_1\bar{X}_0$$

This BE can be more compactly been expressed by using XOR and XNOR gates:

$$\begin{aligned} Y0 &= \bar{X}_3\bar{X}_2(\bar{X}_1\bar{X}_0 + X_1X_0) + \bar{X}_3X_2(\bar{X}_1X_0 + X_1\bar{X}_0) + X_3X_2(\bar{X}_1\bar{X}_0 + X_1X_0) + X_3\bar{X}_2(\bar{X}_1X_0 + X_1\bar{X}_0) \\ &= (\bar{X}_3\bar{X}_2 + X_3X_2)(\bar{X}_1\bar{X}_0 + X_1X_0) + (\bar{X}_3X_2 + X_3\bar{X}_2)(\bar{X}_1X_0 + X_1\bar{X}_0) \\ &= (X_3 XNOR\ X_2)(X_1 XNOR\ X_0) + (X_3 XOR\ X_2)(X_1 XOR\ X_0) \\ &= (X_3 XNOR\ X_2) XNOR (X_1 XNOR\ X_0) \end{aligned}$$

Drawing the circuital schema is now an easy task (left to the reader).

Ex. 5. Design a circuit that, taken two naturals A and B represented with 2 bits, gives in output A+B, if such a number can be represented with 2 bits, otherwise returns the more signifying bits of A+B.

SOLUTION:

a_1	a_0	b_1	b_0	c_1	c_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

The KM for c_1 is:

$a_1\ a_0$ \ $b_1\ b_0$	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	1	1	1	1
10	1	1	1	1

from which $C^1_{min} = a_1 + b_1 + a_0 b_0$, that cannot be further simplified. The KM for c_0 is:

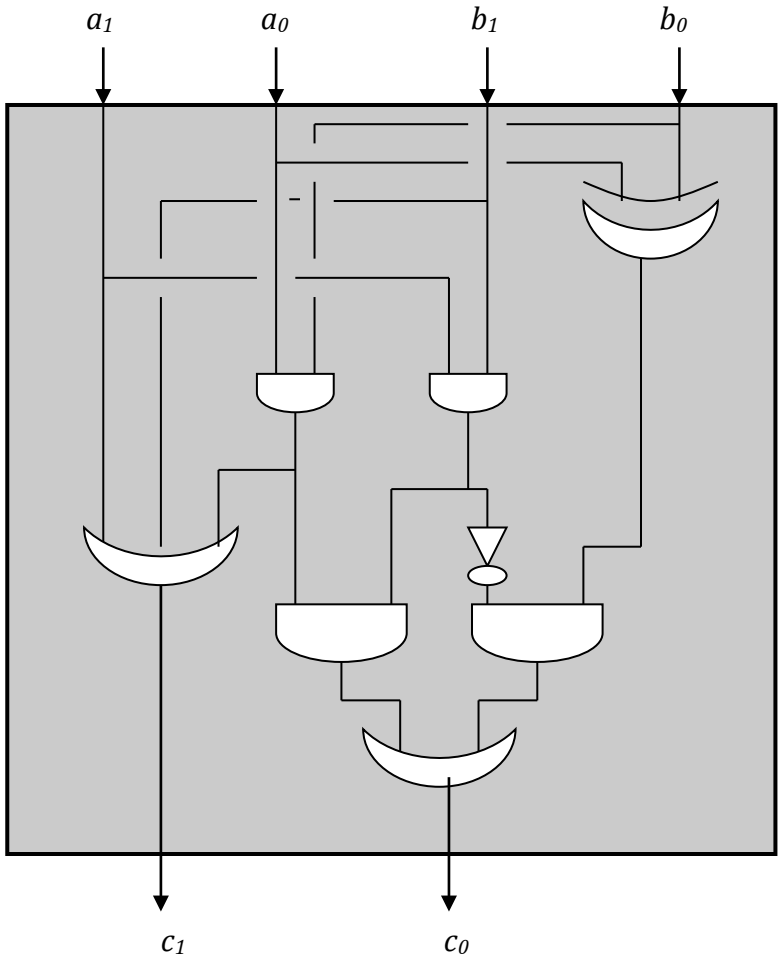
$a_1\ a_0$ \ $b_1\ b_0$	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	1	0
10	0	1	0	0

and so $C^2_{min} = \bar{a}_1 \bar{a}_0 b_0 + \bar{a}_0 \bar{b}_1 b_0 + \bar{a}_1 a_0 \bar{b}_0 + a_0 \bar{b}_1 \bar{b}_0 + a_1 a_0 b_1 b_0$

$= \bar{a}_1 (\bar{a}_0 b_0 + a_0 \bar{b}_0) + \bar{b}_1 (\bar{a}_0 b_0 + a_0 \bar{b}_0) + a_1 a_0 b_1 b_0$

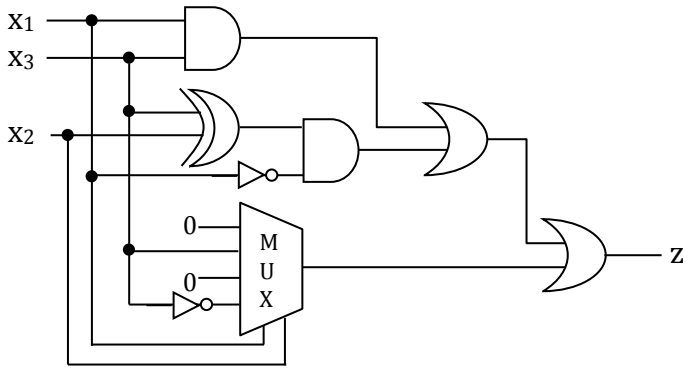
$= (\bar{a}_1 + \bar{b}_1) (a_0 \textbf{ XOR } b_0) + a_1 a_0 b_1 b_0 = \overline{(a_1 \cdot b_1)} (a_0 \textbf{ XOR } b_0) + a_1 a_0 b_1 b_0$

Hence, the circuit is:



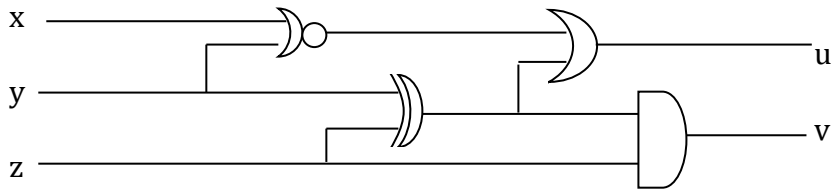
Exercises without solutions

Ex. 1 (REMARK: solve this exercise only after you studied the MSI modules – class 14). Given the circuit:



a) Give the BE for z.
b) From the BE of point a), derive the canonical SOP expresison.
c) Write the minimal POS.
d) Realize z onlt with NAND gates.

Ex. 2. Analyze the following combinatorial circuit:



Then, derive from the BE of *u* its DCF, by using the definition of NOR and XOR and the boolean axioms and laws.

Ex. 3. Given two 2-bits binary numbers A=a1a0 and B=b1b0, design a circuit with 4 input lines a1, a0, b1, b0, and three output lines c2, c1, c0 that calculate:

- A+B if A is smaller than or equal to B
- A-B if A is greater than B

Ex. 4. In the setting of the previous exercise (same input and output bits), design a circuit that calculates:

* A*2 if A+B is odd
* A+B+1 if A+B is even

Ex. 5. Design a circuit with 3 inputs X2X1X0 that outputs Y=1 if and only if X0 = (X1 OR X2) or X1 = (X0 AND X2).

Es. 6. Give a combinatorial circuit such that, given an integer number A with 4 bits represented in 2-complement, returns the integer B such that:

$$B = \begin{cases} A & \text{if A is even} \\ A-1 & \text{if A is odd and positive} \\ A+1 & \text{if A is odd and negative} \end{cases}$$

Assume that A is always different from 1000.