CLASSWORK of COMPUTER ARCHITECTURES -- UNIT 1
February 9th, 2021

Name_____ Surname_____ Matric.numb._____

Exercise 1 (3 points). Prove, by using the Boolean axioms and laws, the following identity:

$$(x + \overline{y}) \cdot \overline{(\overline{x} \cdot y \cdot z)} = \overline{\overline{x} \cdot y}$$

Exercise 2 (5 points) Let A = – 4632,5 x 10^{-2} and B = 13 x 10^{2}. Turn A and B in the IEEE half-precision format. Then, compute A + B and represent the result in the same format. Finally, consider the 16 bits as a single natural binary number, turn it in base 16 and subtract to the result the hexadecimal number 2FD.

Exercise 3 (2+3+3 points) A combinatorial circuit receives in input the binary encoding of a natural number x, with $3 \leq x \leq 15$, and produces in output 3 bits y_2 y_1 y_0 that represent function $y = (3x - 3) \bmod 11$ *(REMARK: Use don't care symbols if y cannot be represented).* Realize the circuit by using a PLA; finally, implement y_1 with a MUX 4-to-1 and y_2 with an ALL-NAND expression.

Exercise 4 (4 points) Design an automaton that receives in input a bit sequence and considers the last 4 bits received as a number in two complement with 4 bits. The output should be:

- A, if such a number is negative but not multiple of 4;
- B, if it is negative and multiple of 4;
- C, if it is positive but not multiple of 4;
- D, otherwise.

REMARK: accept also the sequence 1000, seen as a normal number in two complement. Also assume that the first 3 outputs (at the outset of the automaton) can be any value.

Exercise 5 (2+3 points): Minimize the following automaton, with initial state S0:

	0	1
S0	S2/0	S1/0
S1	S1/0	S3/0
S2	S1/1	S4/0
S3	S3/0	S1/0
S4	S3/1	S4/0

Then, for the minimized automaton, draw the temporal diagram for input 01101.

Exercise 6 (5 points). Consider two source registers S_0 and S_1 and four destination registers D_0, D_1, D_2 and D_3. Design an interconnection such that:

- if S_0 is even, then moves its content into D_0 and D_1; otherwise, it moves its content into D_2.
- If $S_0 + S_1 \geq 0$, then D_3 receives the content of S_1, otherwise the content of S_0.

In both cases, the transfer happens only if S_1 MOD 4 = 0.