Exam of Computer Architectures – UNIT 1 - September 7th, 2021

Exercise 1 (3 points): Turn into base 5, by showing all steps, the following number in base 10: 120,15.

Exercise 2 (3 points): Sum the following numbers in IEEE half-precision format:
< 0 ; 01010 ; 1110000000 > and < 1 ; 10000 ; 1100000000 >

Exercise 3 (2 points): Draw the circuit schema of a downwards synchronous counter modulo 32.

Exercise 4 (2+2+2+1 points):
a) Write the truth table of the function that, taken a 3 bits integer (in 2-complement), returns its double represented as a 4 bits integer (in 2-complement). Assume that 100 will never be received.

b) Implement the most signifying bit of the obtained function with a MUX 2-to-1:

c) Write the minimal POS formulae associated to the two less signifying bits of the function:

d) Implement the whole function with a ROM:

Exercise 5 (6 points): Consider the following automaton:

	0	1
S0	S1/0	S0/0
S1	S2/0	S3/1
S2	S2/0	S3/1
S3	S1/0	S0/1
S4	S1/0	S5/0
S5	S2/0	S4/0

Minimize it and write down the associated sequential net that uses a JK FF for the most signifying bit and a T FF for the less signifying one.

Exercise 6 (4 points): Design an automaton that receives in input two bit sequences and gives in output 1 whenever the last three bits of the first sequence followed by the last two bits of the second sequence represent a natural number in base 2 that is a multiple of 8. The first two outputs are ignored, hence you can handle them in the way that makes the automaton simpler.

Exercise 7 (5 points): We have four source registers S_0, S_1, S_2 and S_3 and two destination registers D_0 and D_1. Implement an interconnection such that:

- The index of the source register to be moved into D_0 is given by calculating $(S_0+2) \bmod 4$;
- D_1 receives the content of S_1, if S_0 is greater than or equal to S_2; S_3 otherwise.

In both cases, trasfers are enabled only if S_3 is even.