Exam of Computer Architecture Unit 1 – June 28th, 2022

Exercise 1 (2+2+2+2 points) Given X in 2 complement with 4 bits,

- Give the truth table for the Boolean function Y, represented in 2 complement with 4 bits $y_3y_2y_1y_0$, such that:

$$Y = \begin{cases} 12 - 2X & \text{if } X \text{ is even} \\ 2X + 9 & \text{if } X \text{ is odd} \end{cases}$$

  Use *don't care* symbols for the values of Y that are not representable with 4 bits;
- Implement Y by using a PLA;
- Implement y_2 by using a MUX 4-to-1;
- Provide an ALL-NAND expression for y_2.

Exercise 2 (7 punti) Design a sequential net that receives in input a sequence of characters chosen from the alphabet {A, E, G, M} and produces in output 1 whenever it recognizes sequences GAG and GAME, also with overlapping. Provide the automaton *(3 points)* and the futurte states table, by using a JK FlipFlop for the MSB and a SR FlipFlop for the LSB *(2 points)*. Finally, derive the minimal expressions *(2 punti)*.

Exercise 3 (3 points) Prove the following identity, by specifying the axioms and rules of the Boolean algebra used in every step:

$$c + \overline{(a + (b \oplus c))} + c = a + b + c$$

Exercise 4 (4 points) Given A= -34,83, represent it in floating point by using the IEEE half-precision format. Then, compute the sum between A and B = <0;10011; 1011011000> and represent the result in the same floating point format. Finally, turn into hexadecimal the binary number obtained from the 16 bits of the IEEE half-precision representation of the result.

Exercise 5 (3 points) Minimize the following automaton:

	0	**1**
A	B/0	C/0
B	A/0	C/1
C	B/1	A/1
D	B/0	E/0
E	B/1	D/1
F	G/0	E/1
G	F/0	C/0

Exercise 6 (5 points). Consider the four source registers $S_0 - S_3$ and the three destination registers $D_1 - D_3$. Design an interconnection net such that:

- D_3 receives the content of $S_{(i+1) \text{ MOD } 4}$, where index *i* is given by the two most signifying bits of S_2;
- Moves the XOR between S_2 and S_3 into D_1, if the content of S_1 is odd, or into D_2, otherwise.

The transfers are enabled if the difference between S_2 and S_3 is negative.