Classwork of Computer Architecture UNIT 1 - 1/2/2022 **(A)**

Exercise 1 (4 points): Consider the source registers R0, R1 and R2, and the destination registers D0, D1, D2 and D3. Design an interconnection schema such that:

- in D0 is moved R0, if R0 itself is even, otherwise it is moved the opposite of R0;
- the sum between R1 and R2 is moved in D1 if R2> R1, in D2 if R2<R1, in D3 if R1=R2.

Transfers are enabled if R1 and R2 are even and with different sign.

Exercise 2 (3 points): By using axioms and laws of Boolean algebra, prove the following identity:

$$\left(a\bar{b} + \overline{\bar{b}c + c(\bar{a} + b)}\right) \oplus ac = ab + \bar{c}$$

Exercise 3 (10 points): Give the tabular representation of an automaton that receives in input a bit sequence and gives in output 1 whenever the last 3 bits, seen as an integer in 2-complement, represent a negative number that is not multiple of 4, by also considering overlappings; when 3 bits have not been received yet, return 0. Then, draw the temporal diagram with input 11001. Finally, modify the automaton not to admit overlappings, minimize it and synthetize the associated circuit, by using a JK FF for the most signifying bit, T FFs for the remaining bits, and a PLA for the combinatorial part.

Exercise 4 (5 points): Consider the hexadecimal number 2A5B and subtract to it in base 16 the hexadecimal number 9C7. Then, convert the result in a binary sequence of 16 bits, to be considered as a rational number in IEEE 754 half-precision format. Subtract from this number the rational number <1;01001;1100000000>, still expressed in IEEE half-precision format, and write the result in the same format.

Exercise 5 (1+1+2+2+2 points): The 4 variables function $f(a,b,c,d)$ holds 0 if $a(b \oplus c)=1$ or if $a+b+d=0$.

- Provide the truth table for f
- Write the canonical SOP and POS expressions for f
- Write the minimal SOP and POS expressions for f
- Realize f by using a MUX with 4 inputs
- Write f in ALL-NAND form

Classwork of Computer Architecture UNIT 1 - 1/2/2022 **(B)**

Exercise 1 (1+1+2+2+2 points): The 4 variables function $f(a,b,c,d)$ holds 0 if $(\bar{a}+b)(a+\bar{b})$=1 or if $a \oplus b \oplus d$=0.

- Provide the truth table for f
- Write the canonical SOP and POS expressions for f
- Write the minimal SOP and POS expressions for f
- Realize f by using a MUX with 4 inputs
- Write f in ALL-NOR form

Exercise 2 (4 points): Consider the source registers R0, R1 and R2, and the destination registers D0, D1, D2, D3 and D4. Design an interconnection schema such that:

- in D0 is moved R0-R1, if R2 is even, otherwise it is moved R1-R0;
- R2 is moved in D1, if R1 is even and non-negative, in D2, if R1 is odd and non-negative, in D3, if R1 is even and negative, in D4, if R1 is odd and negative.

Transfers are enabled if R0 is not multiple of 2.

Exercise 3 (10 points): Give the tabular representation of an automaton that receives in input a bit sequence and gives in output 1 whenever the last 3 bits, seen as an integer in 2-complement, represent a number that is either negative or multiple of 4, by also considering overlappings; when 3 bits have not been received yet, return 0. Then, draw the temporal diagram with input 11001. Finally, modify the automaton not to admit overlappings and synthetize the associated circuit, by using a JK FF for the most signifying bit, T FFs for the remaining bits, and a PLA for the combinatorial part.

Exercise 4 (3 points): By using axioms and laws of Boolean algebra, prove the following identity:

$$\left(x\bar{z} + \overline{yz + y(x+\bar{z})}\right) \oplus xy = \bar{y} + xz$$

Exercise 5 (5 points): Consider the hexadecimal number 4A5B and subtract to it in base 16 the hexadecimal number 6C1. Then, convert the result in a binary sequence of 16 bits, to be considered as a rational number in IEEE 754 half-precision format. Subtract from this number the rational number <1;10001;1110000000>, still expressed in IEEE half-precision format, and write the result in the same format.