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DIPARTIMENTO DI INFORMATICA

Synthesis of combinatorial nets (all methods)

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Specification

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Realize in all possible ways (logical gates, ROM, PLA and MUX of all possible sizes) a circuit that computes the opposite of a 4 bits integer represented 2 complement.

This sequence is not used in 2 compl. because its opposite is not representable in the specified format

$x_3\,x_2\,x_1\,x_0$	$y_3\,y_2\,y_1\,y_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 0
0 0 1 1	1 1 0 1
0 1 0 0	1 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	- - - -
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 0 1 0
1 1 1 1	0 0 0 1

ROM

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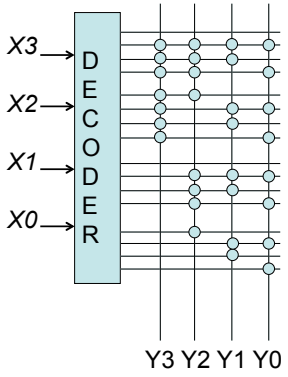
$x_3\,x_2\,x_1\,x_0$	$y_3\,y_2\,y_1\,y_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 0
0 0 1 1	1 1 0 1
0 1 0 0	1 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	- - - -
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 0 1 0
1 1 1 1	0 0 0 1



Logic gates

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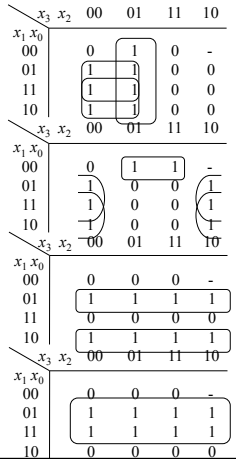
$x_2\,x_2\,x_1\,x_0$	$y_3\,y_2\,y_1\,y_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 0
0 0 1 1	1 1 0 1
0 1 0 0	1 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	- - - -
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 0 1 0
1 1 1 1	0 0 0 1



y3 = x3x2+x3x1+x3x0
= x3(x2+x1+x0)

y2 = x2x0+x2x1+x2x1x0
= x2(x0+x1)+x2x1x0
= x2 XOR (x1+x0)

y1 = x1x0+x1x0
= x1 XOR x0

y0 = x0

PLA

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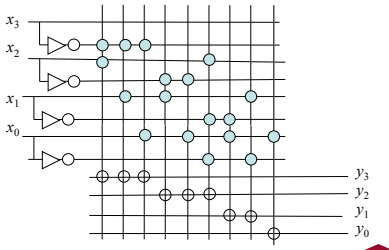
$x_3\,x_2\,x_1\,x_0$	$y_3\,y_2\,y_1\,y_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 0
0 0 1 1	1 1 0 1
0 1 0 0	1 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	- - - -
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 0 1 0
1 1 1 1	0 0 0 1

y3 = x3x2+x3x1+x3x0

y2 = x2x0+x2x1+x2x1x0

y1 = x1x0+x1x0

y0 = x0



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MUX

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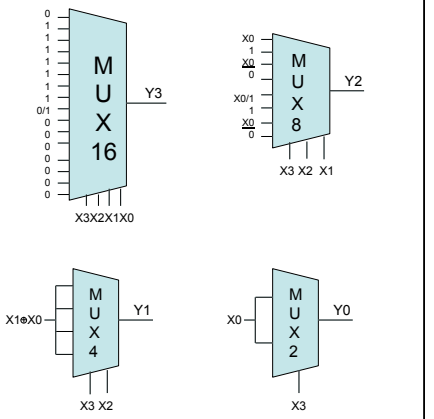
$x_3\,x_2\,x_1\,x_0$	$y_3\,y_2\,y_1\,y_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 0
0 0 1 1	1 1 0 1
0 1 0 0	1 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	- - - -
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 0 1 0
1 1 1 1	0 0 0 1



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Comparison

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ROM: - DECOD 4-to-16: 4 NOT
16 4-ary AND = 48 AND
- 1 diod for every "1" → 7+8+8+8 = 31
TOTAL: 83 gates/diods

Gates: 1 NOT + 1 AND + 2 OR (one is used twice) + 2 XOR = 6 gates

PLA: 4 NOT + 9 AND + 5 OR = 18 gates

MUX: - MUX 16-to-1 = 52 (DEC 4-to-16) + 16 AND + 15 OR
- MUX 8-to-1 = 19 (DEC 3-to-8) + 8 AND + 7 OR
+ 1 NOT to realize the input function
- MUX 4-to-1 = 6 (DEC 2-to-4) + 4 AND + 3 OR
+ 1 XOR for the input function
- MUX 2-to-1 = 1 (DEC 1-to-2) + 2 AND + 1 OR
TOTAL = 83+35+14+4 = 136 gates

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