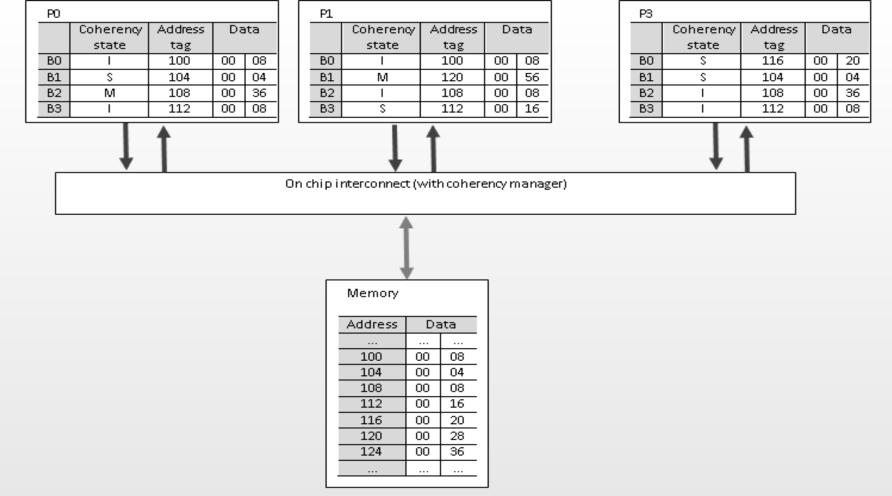
Advanced Parallel Architecture

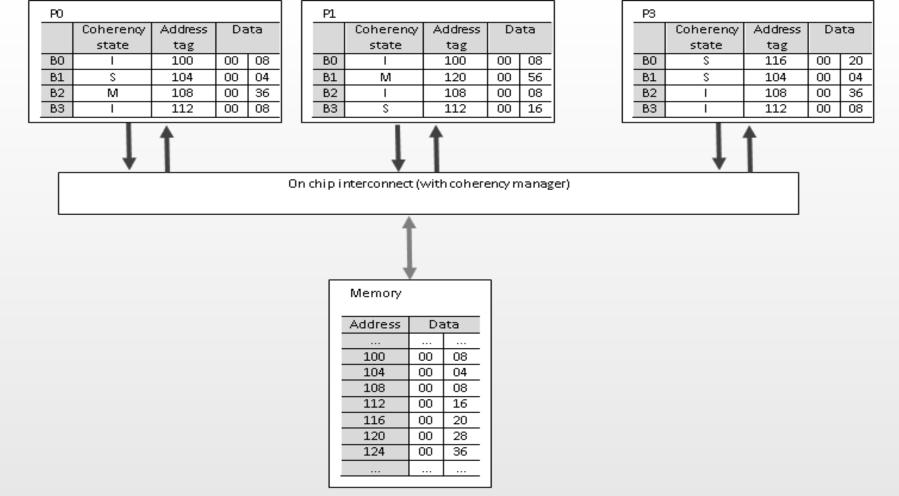
Annalisa Massini - 2016/2017

Cache Coherence: Exercises

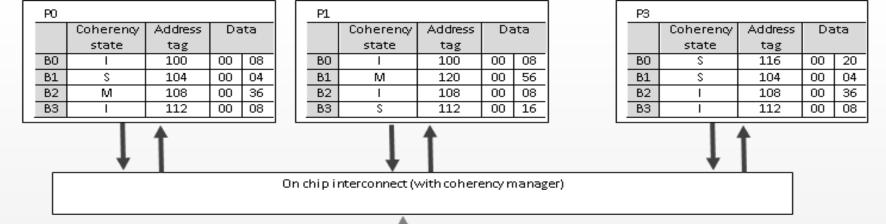
Advanced and Parallel Architectures 2016/2017



- Consider a multicore multiprocessor implemented as a symmetric sharedmemory architecture
- Each processor has a single, private cache
- Coherence is maintained using the snooping coherence protocol

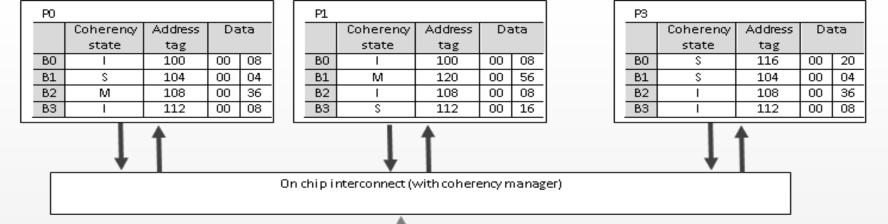


- Each cache is direct-mapped, with **four blocks** each holding **two words**
- > The coherence **states** are denoted **M**, **S**, and **I** (Modified, Shared, and Invalid)



- P# designates the CPU (e.g., PO)
- > <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

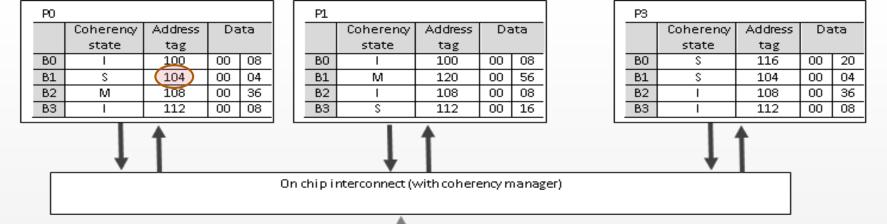
	,		
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	



- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

+			
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



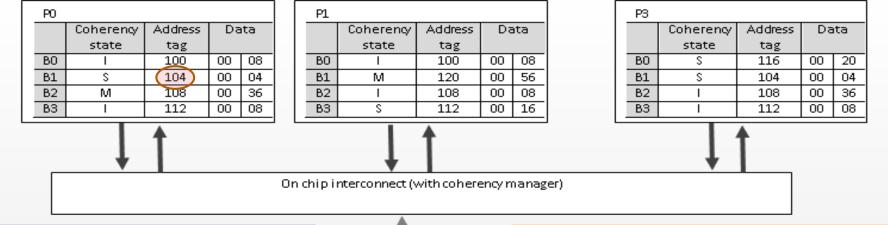
- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Memory		
Address	Da	ata
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Exercise 5 - June 11th, 2015

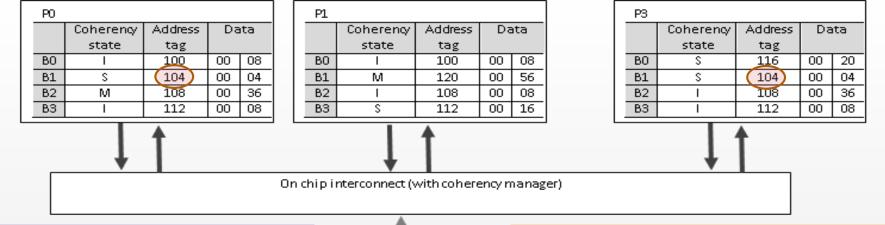


- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action **P0: write 104 ← 24**

	,		
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



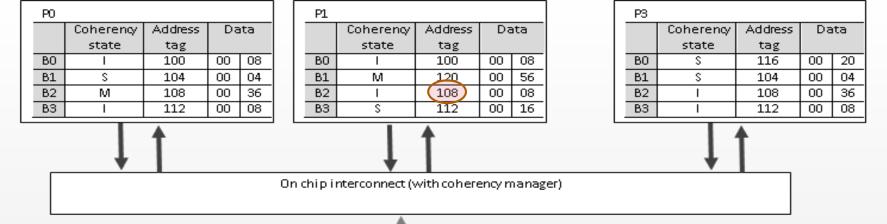
- **P#** designates the CPU (e.g., P0)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a **write** operation

PO· write $104 \leftarrow 24$

Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P0: write 104	← 24	
	hit/miss	state before	Pi.Bj (state, tag, datawords)
	HIT	S	P0. B1 (M, 104, 00 24)
		S	P3. B1 (I, 104, 00 04)

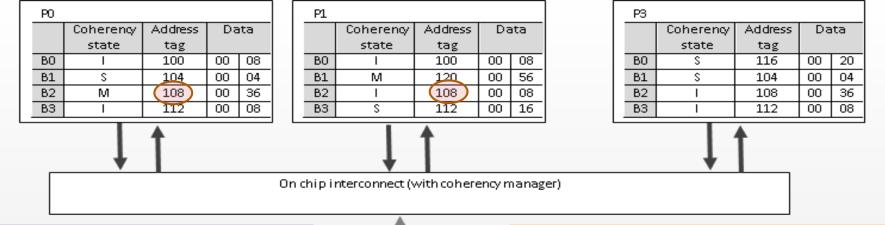


- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action P1: read 108

	-		
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

1 4 0 0

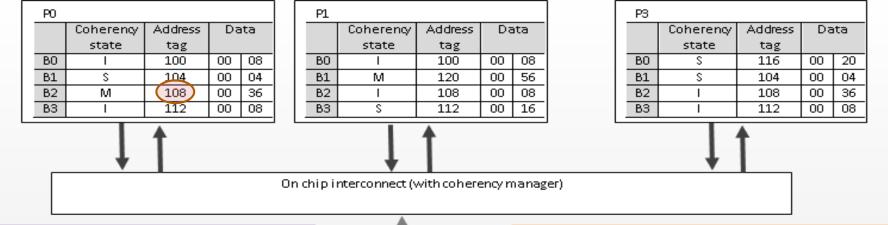
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P1: read 108			
	hit/miss	state bef	fore	Pi.Bj (state, tag, datawords)
	MISS	1		P1. B2 (S, 108, 00 36)
		Μ		P0. B2 (S, 108, 00 36)
	Deturneducelus	here we ded	00.00	
	Returned value	by read	00 36	

Advanced and Parallel Architectures 2016/2017

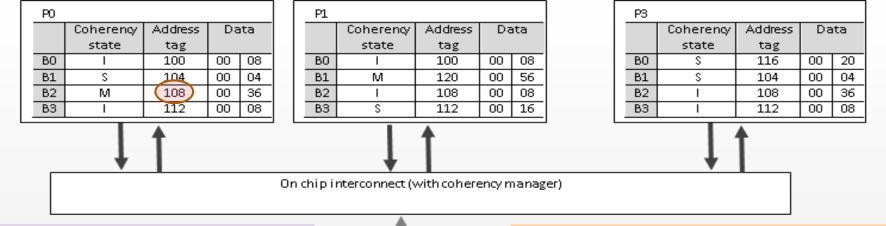


- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action **P0: write 124 ← 12**

	,		
Memory			
Address	Da	ata	
100	00	08	
104	00	04	
108	00	08	
112	00	16	
116	00	20	
120	00	28	
124	00	36	

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Memory		
Address	Da	ata
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36

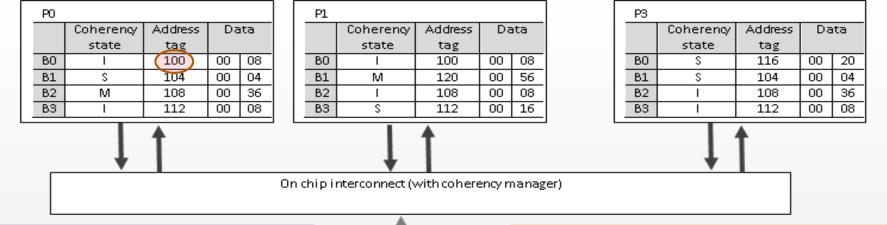
For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 124 ← 12**

hit/miss	state before
MISS	Μ

Pi.Bj (state, tag, datawords) P0. B2 (M, 124, 00 12) *memory (108, 00 36)*

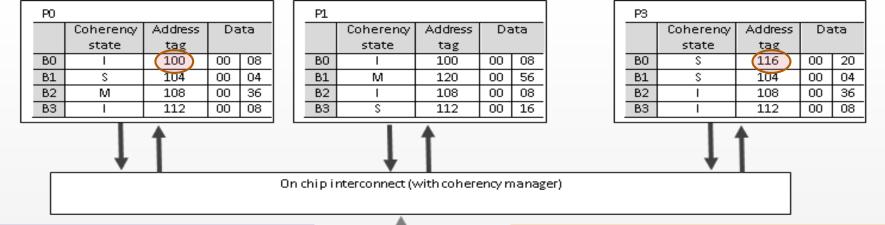


- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action **P0: write 116 ← 32**

Memory												
Address	ss Data											
100	00	08										
104	00	04										
108	00	08										
112	00	16										
116	00	20										
120	00	28										
124	00	36										

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



- **P#** designates the CPU (e.g., P0)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Memory												
Address	Iress Data											
100	00	08										
104	00	04										
108	00	08										
112	00	16										
116	00	20										
120	00	28										
124	00	36										

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P0: write 116	← 32		
	hit/miss MISS	stat M	e before	Pi.Bj (state, tag, datawords) P0. B0 (M, 116, 00 32)
		S		P3. B0 (I, 116, 00 20)

				P1					P2					P3				
Coherency	Address	Da	ata		Coherency	Address	Da	ata		Coherency	Address	Da	ita		Coherency	Address	Da	ata
state	tag				state	tag				state	tag				state	tag		
S	116	00	20	BO	I	100	00	08	BO	S	116	00	20	BO	М	100	00	24
м	120	00	32	B1	I	120	00	28	B1	I	120	00	28	B1	1	120	00	28
I	124	00	12	B2	м	124	00	20	B2	M	108	00	36	B2	1	108	00	32
S	112	00	16	B3	S	112	00	16	B3	S	112	00	16	B3	S	112	00	16
On chip interconnect (with											jer)				ļ			
	state S	state tag S 116 M 120 I 124	state tag S 116 00 M 120 00 I 124 00	state tag S 116 00 20 M 120 00 32 I 124 00 12	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12	Coherency state Address tag Data Coherency state Coherency state S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency state Address tag Data Coherency state Address tag S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency state Address tag Data Coherency state Address tag Data S 116 00 20 B0 I 100 00 M 120 00 32 B1 I 120 00 S 112 00 16 B3 S 112 00	Coherency state Address tag Data Coherency state Address tag Data S 116 00 20 B0 I 100 00 08 M 120 00 32 B1 I 120 00 28 S 112 00 16 B3 S 112 00 16	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency state Address tag Data tag Coherency state Address tag Data tag Coherency state Address tag Data S 116 00 20 B0 1 100 00 08 M 120 00 32 B1 1 120 00 28 S 112 00 12 B2 M 124 00 20 S 112 00 16 B3 S 112 00 16	Coherency state Address tag Data Coherency state Address tag S 116 00 20 B0 I 100 00 08 B0 S 116 110 100 00 08 B1 I 120 00 28 B1 I 120 12 120 12 <td< td=""><td>Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16</td><td>Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16</td><td>Coherency Address Data state tag </td><td>Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16</td><td>Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16</td><td>Coherency Address Data state tag </td></td<>	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency Address Data state tag	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency state Address tag Data S 116 00 20 M 120 00 32 I 124 00 12 S 112 00 16	Coherency Address Data state tag

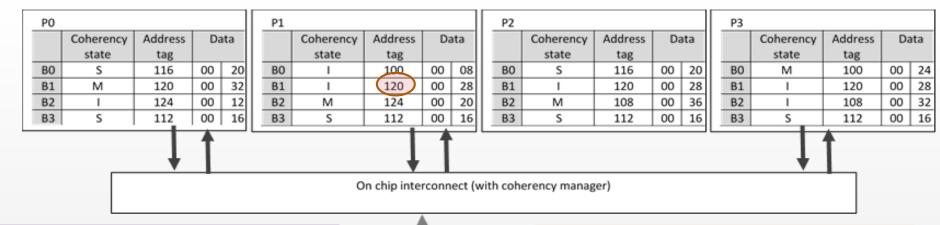
- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

	r -											
Memory												
Address	s Data											
100	00	08										
104	00	04										
108	00	08										
112	00	16										
116	00	20										
120	00	28										
124	00	36										

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Exercise 4 - June 26th, 2015

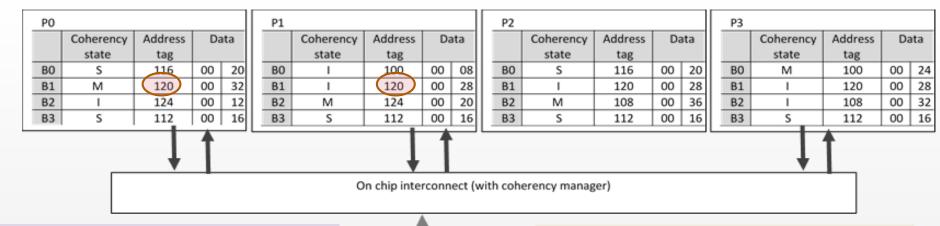


- P# designates the CPU (e.g., PO)
- **<op>** is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action **P1: write 120 ← 24**

	7	
Memory		
Address	Da	ta
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

	r										
Memory											
Address	Data										
100	00	08									
104	00	04									
108	00	08									
112	00	16									
116	00	20									
120	00	28									
124	00	36									

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P1: write 120	~ 24	
	hit/miss MISS	state before I M	Pi.Bj (state, tag, datawords) P1. B1 (M, 120, 00 24) P0. B1 (I, 120, 00 32)

PO					P1					Р	2					P3				
	Coherency	Address	Da	ata		Coherency	Address	Da	ata		Т	Coherency	Address	Da	ita		Coherency	Address	Da	ita
	state	tag				state	tag					state	tag				state	tag		
BO	S	116	00	20	BO	I	100	00	08	В	0	S	116	00	20	BO	м	100	00	24
B1	м	120	00	32	B1	I	120	00	28	В	1	I	120	00	28	B1	1	120	00	28
B2	I	124	00	12	B2	м	124	00	20	В	2	м	108	00	36	B2	1	108	00	32
B3	S	112	00	16	B3	S	112	00	16	В	3	S	112	00	16	B3	S	112	00	16
On chip interconnect (with co											oher	rency manag	er)				ļ	1		

- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action P3: read 108

1	7	
Memory		
Address	Da	ta
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

PO					P1					P2					P3				
	Coherency	Address	Da	ita		Coherency	Address	Da	ata		Coherency	Address	Da	ata		Coherency	Address	Da	ata
	state	tag				state	tag				state	tag				state	tag		
BO	S	116	00	20	BO	I	100	00	08	BC	S	116	00	20	BO	м	100	00	24
B1	M	120	00	32	B1	I	120	00	28	B1	1	120	00	28	B1	1	120	00	28
B2	I	124	00	12	B2	м	124	00	20	B2	M	108	00	36	B2	1	108	00	32
B3	S	112	00	16	B3	S	112	00	16	B3	S	112	00	16	B3	S	112	00	16
	$\begin{array}{c c c c c c c c c c c c c c c c c c c $																		
On chip interconnect (with coherency manager)																			

- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

	r	
Memory		
Address	Da	ta
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P3: read 108			
	hit/miss MISS	state before I M	Pi.Bj (state, tag, datawords)P3. B2 (S, 108, 00 36)read 3P2. B2 (S, 108, 00 36)	6

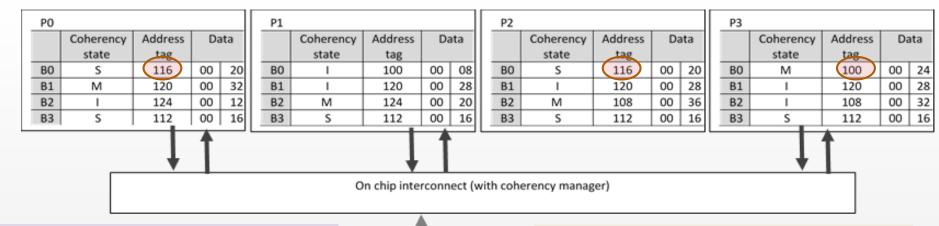
PO					P1					Γ.	P2					P3		_		
	Coherency	Address	Da	ata		Coherency	Address	Da	ata	H		Coherency	Address	Da	ata		Coherency	Address	Da	ita
	state	tag				state	tag			L I		state	tag				state	tag		
BO	S	116	00	20	BO	1	100	00	08		BO	S	116	00	20	BO	м	100	00	24
B1	м	120	00	32	B1	1	120	00	28		B1	I	120	00	28	B1	1	120	00	28
B2	I	124	00	12	B2	м	124	00	20	H	B2	м	108	00	36	B2	I	108	00	32
B3	s	112	00	16	B3	S	112	00	16	H	B3	S	112	00	16	B3	S	112	00	16
		ļ	1			O	n chip inte	rconn	ect (v	with	h coh	erency manag	ger)				ļ			

- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

Action **P2: write 100 ← 20**

+							
Memory							
Address	Da	ta					
100	00	08					
104	00	04					
108	00	08					
112	00	16					
116	00	20					
120	00	28					
124	00	36					

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



- P# designates the CPU (e.g., PO)
- <op> is the CPU operation (e.g., read or write)
- <address> denotes the memory address
- <value> indicates the new word to be assigned on a write operation

+							
Memory							
Address	Da	ta					
100	00	08					
104	00	04					
108	00	08					
112	00	16					
116	00	20					
120	00	28					
124	00	36					

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action	P2: write 10	0 ← 20	
	hit/miss	state before	Pi.Bj (state, tag, datawords
	MISS	S	P2. B0 (M, 100, 00 20)
		S	P0. B0 (M, 116, 00 20)
		Μ	P3. B0 (I, 100, 00 24)

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