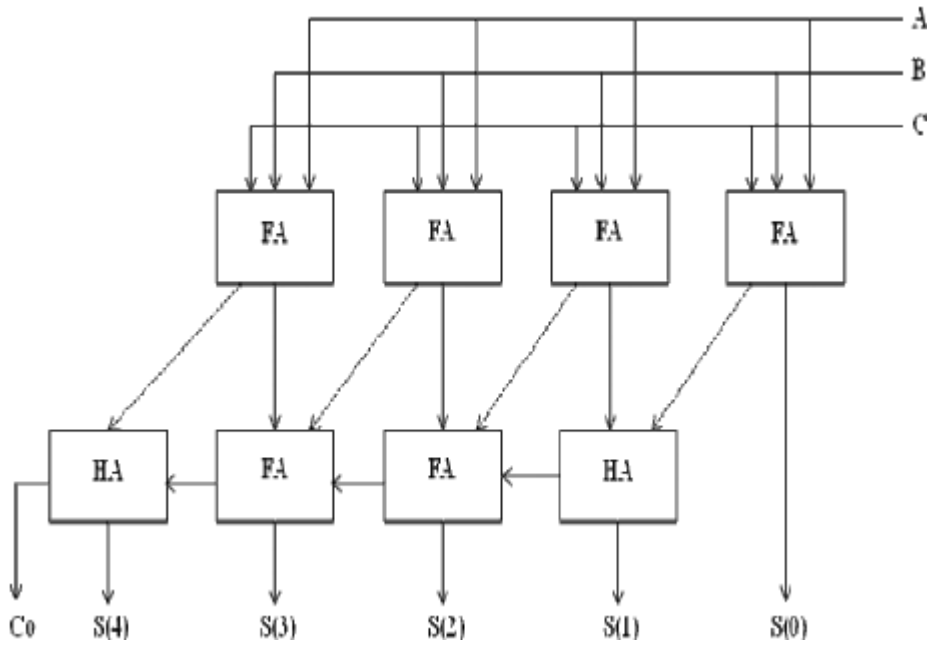
Exercise 3 (4 points) - Circuit time and area **APA course -13 June 2017 – Part A**

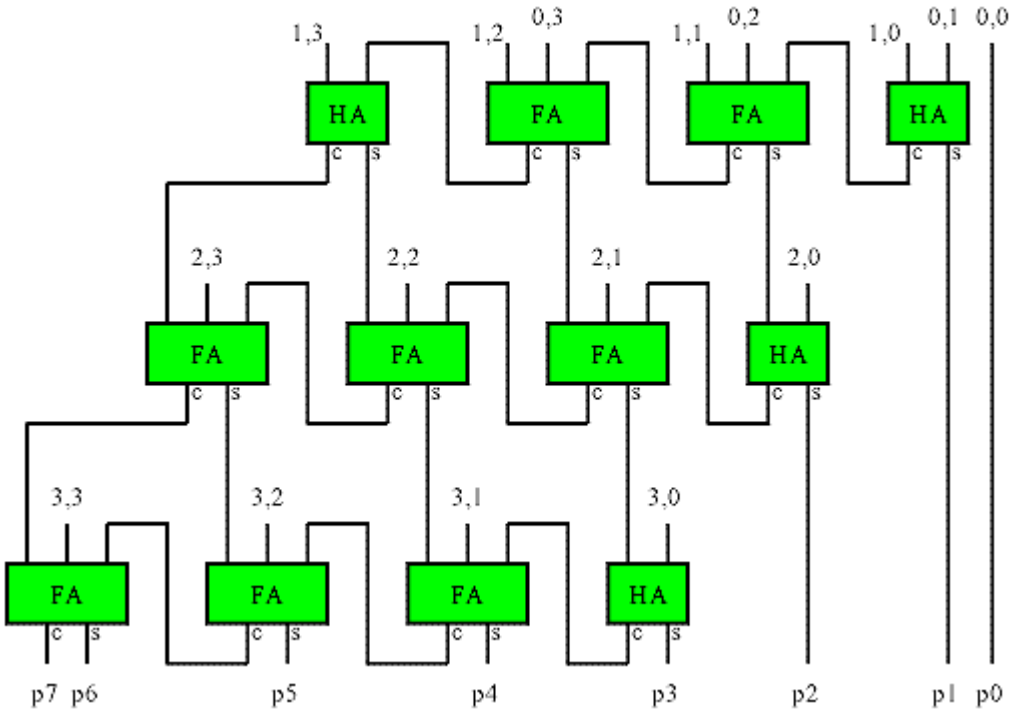
Compute the **time** (propagation delay) and **area** required by the 4-bits Carry-Save-Adder, that is an adder for three values A, B and C, shown here below.

Compute the **speedup** of 4-bits Carry-Save-Adder with respect to the standard binary ripple-carry adder.



Exercise 6 (4 points) - Circuit time and area **APA course - 7 December 2018 – Part A**

Compute the **time** (propagation delay) and **area** required by the 4-bits **ripple carry array multiplier**, shown here below.

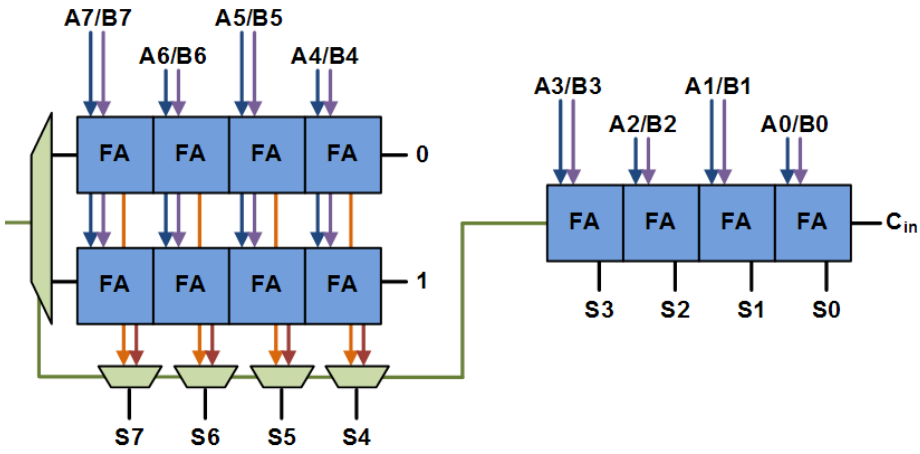


Exercise 3 (3+2 points) - Circuit time and area **APA course – 5 July 2017 – Part A (a)**

A particular way to implement an adder is given by the ***carry-select adder***, generally consisting of ripple carry adders and multiplexers. A 8-bit carry-select adder with a uniform block size of 4 is shown in the figure.

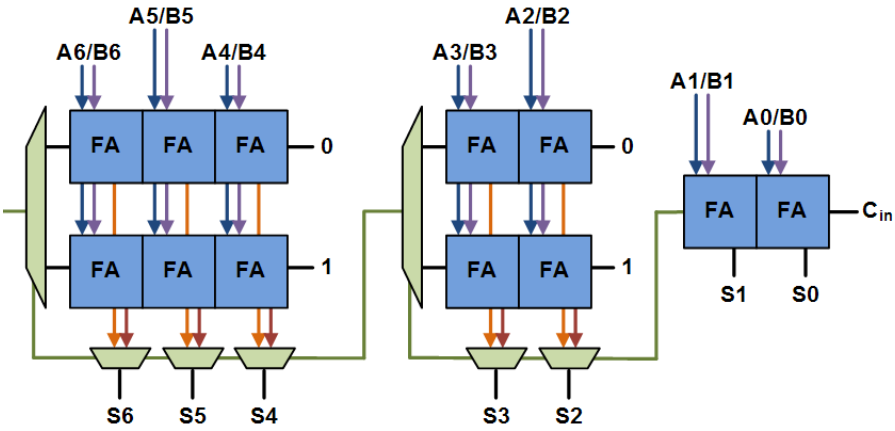
i) Compute the ***time*** (propagation delay) and ***area*** required by the 8-bit carry-select adder.

ii) Compare the 8-bits carry-select adder and the standard binary ripple-carry adder (that is compute the **speedup** both for time and area).



Exercise 3 (3+2 points) - Circuit time and area **APA course – 5 July 2017 – Part A (b)**

A particular way to implement an adder is given by the ***carry-select adder***, generally consisting of ripple carry adders and multiplexers. A 7-bit carry-select adder with a variable block size is shown in the figure.



i) Compute the ***time*** (propagation delay) and ***area*** required by the 7-bit carry-select adder.

ii) Compare the 7-bits carry-select adder and the standard binary ripple-carry adder (that is compute the **speedup** both for time and area).