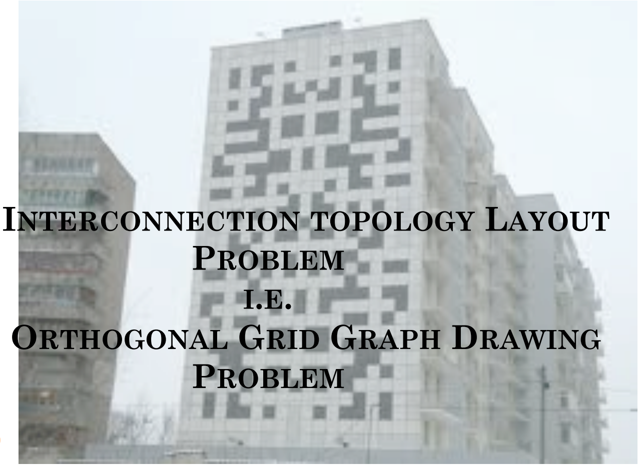


THE INTERCONNECTION TOPOLOGY LAYOUT PROBLEM
I.E.
THE ORTHOGONAL GRID GRAPH DRAWING PROBLEM

Prof. Tiziana Calamoneri
Network Algorithms
A.A. 2013/14

THOMPSON'S MODEL

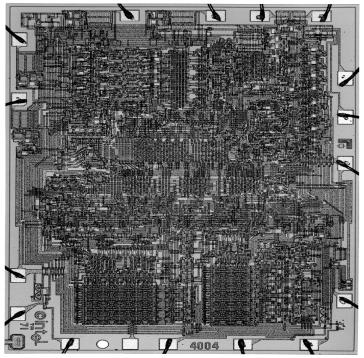
THOMPSON'S MODEL (1)

- The interconnection topology *layout problem* arises from the problem of producing efficient VLSI (Very Large Scale Integration) layouts on a silicon board.
- It was born in the '40s, but it got a significative interest only relatively recently, when the technology has allowed to layout circuits in two and three dimensions at reasonably low price.

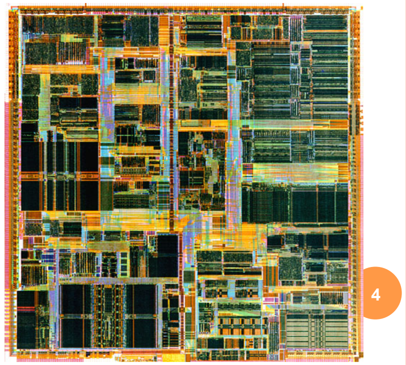
THOMPSON'S MODEL (2)

Two exemples of VLSI circuits:

Intel 2004



Intel Pentium



Thompson's Model (3)

Model the circuit as a graph (nodes = ports, switches, etc. and edges = wires).

There is a tight relation between the VLSI layout and the graph drawing.

Drawing *Γ* of a graph *G*: it is a function mapping each node *v* in a distinct point *Γ(v)*, and each edge *(u,v)* in an open Jordan curve *Γ(u,v)* not crossing any point that is the mapping of a node, starting in *Γ(u)* and arriving in *Γ(v)*.

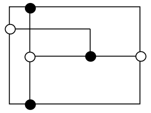
The VLSI technology production imposes many constraints; in particular, we have to keep into account the following:

- …

Thompson's Model (4)

- … the device pressing the connections can only approximate slanting lines by tiny horizontal and vertical segments (⇒orthogonal drawing);

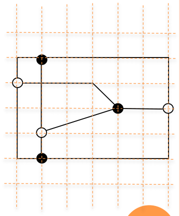
Orthogonal drawing: drawing of a graph where edges are represented as broken lines whose segments are horizontal or vertical (parallel to the coordinate axes)



Thompson's Model (5)

- In order to avoid interference, it is necessary to keep wires far enough (⇒grid drawing);

Grid drawing: drawing of a graph so that all nodes, crosses and bends of the edges are put on grid points
(scaling property - resolution)



Thompson's Model (6)

- Wires cannot cross; in order to avoid crossings, it is possible to route the crossing wires on the two separate sides of the board, introducing small “holes” trepassing the board from a side to the other one; the number of such holes must be small, as their realization is rather expensive (⇒crossing number minimization)
- …

Thompson's Model (7)

- The silicon is very expensive; so the layout must have small area (⇒area minimization).
- Wires should not be too long, as the propagation delay is proportional to their length; in case of layered topology, wires in the same layer should have (approximately) the same length, so to avoid synchronization problems (⇒edge length minimization).

Thompson's Model (8)

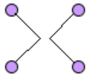
In 1980 Thompson introduced a model that is consistent with all the mentioned constraints:

the layout of a topology *G* is a plane representation on a bunch of unit distance horizontal and vertical traces that maps:

…

Thompson's Model (9)

- nodes of *G* in the intersecion points of the traces,
- edges of *G* in disjoint paths constituted by horizontal and vertical segments on traces; such paths cannot cross nodes that are not their extremes and they can cross each other only in corrispondence of trace intersection points;
- Overlappings (edge-edge) are not allowed
- Node-edge crosses are not allowed
- "knock-knees" are not allowed



Ortoghonal Graph Drawing

Orthogonal Grid Drawing (1)

- DEF. An *orthogonal grid drawing* of a graph $G=(V,E)$ is a bijection mapping:
  - nodes $v \in V$ on plane points $\Gamma(v)$ at integer coordinates
  - edges $(v,w) \in E$ on not overlapping paths so that the images of their extremes $\Gamma(v)$ and $\Gamma(w)$ are connected by the corresponding paths.
  - These paths are constituted by horizontal and vertical segments; the possible bends have integer coordinates
- Obs. only graphs with degree ≤ 4 can be correctly drawn.

Orthogonal Grid Drawing (2)

- So, the interconnection topology layout is an orthogonal grid drawing of the corresponding graph with the aim of minimizing the area, the number of crossings and the wire length.
- There is a huge literature in the GRAPH DRAWING area…
- Shall we use the known algorithms for orthogonal grid drawing in order to solve the layout problem?

Orthogonal Grid Drawing (3)

- No: these algorithms guarantee some bounds on the optimization functions that hold FOR EACH input graph having the required input hypotheses
- Interconnection topologies are very structured graphs (usually regular, symmetric, recursively built, …) and, exploiting these properties, it is possible to get better results.

Orthogonal Grid Drawing (4)

- Graph drawing algorithms get a graph in input and draw it on the plane.
- Layout algorithms are designed for a single special interconnection topology and so they get only its dimension in input.
- Obs. Improving an optimization function by “only” a constant factor is an important issue (especially the area): if a layout occupies ½ of the area of another one, it will cost the half!

Butterfly Layout

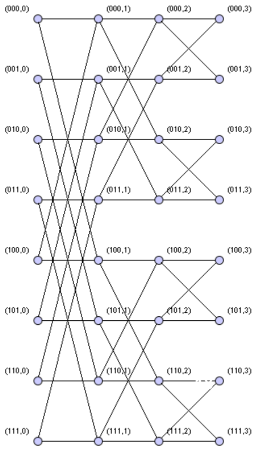
Butterfly Network (memorandum)

Def. (reminder) Let $N=2^n$ (and $n=log\ N$); an n-dimensional Butterfly is a layered graph having $N\ (n+1)$ nodes ($n+1$ layers, with 2^n nodes each) and $2Nn$ edges.

The nodes are labeled with a pair (w, i), where i is the *layer* of the node and w is an n bit binary number indicating the row of the node.

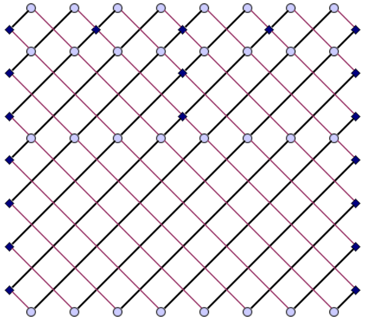
Two nodes (w, i) and (w', i') are adjacent iff $i'=i+1$ and:

- $w=w'$ (*straight edge*) or
- w e w' differ in exactly the i-th bit (*cross edge*).



Wise Layout (1)

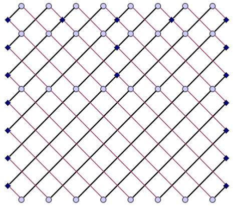
Layout proposed by D.S.Wise ['81]



He writes:

"This paper offers a result that can be described as a picture. […] The perceptive reader may stop here, since the remainder of this paper only describes it."

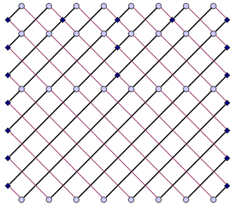
Wise Layout (2)



This layout has a property that is very important in a layered topology:

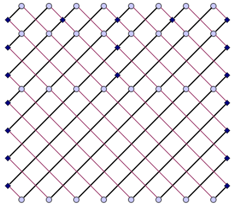
- All the wires in the same layer are of equal length.
- Nevertheless, this length grows exponentially up with the layer.

Wise Layout (3)



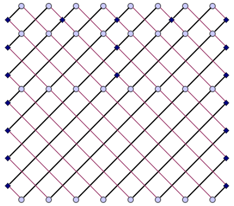
- The longest path length from any input to any output is linear in N (namely, $2(N-1)$).
- Indeed:
  - All the paths have the same length.
  - For the sake of simplicity, consider the path from the upper-left node to the lower-right node.
  - The length of this path coincides with the diagonal of the square having side $\sqrt{2}\,(N-1)$, so it is $2(N-1)$.

Wise Layout (4)



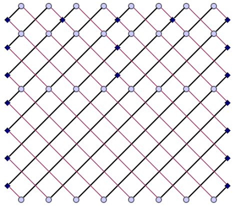
- The layout is performed on the two sides of the silicon board, so it can be considered a 2-layer layout; one layer is composed of all diagonal wires running "north-east" (from lower-left to upper-right) -red lines- and the other layer is composed of "north-west" wires (from lower-right to upper-left) -black lines.

Wise Layout (5)



- PROs:
  - Good area : $\sqrt{2}\,(N-1) \times \sqrt{2}\,(N-1)= 2N^2+o(N^2)$
  - Constant wire length on each layer; this is not true in every layout: in the classical drawing of the butterfly network, for example, the straight-edges on the last layer have unit length while the cross-edges on the same layer have linear length in the input size N; this is extremely bad, because synchronization of the information flow goes lost;
  - The input and output nodes lie on the boundary of the layout, and this can be required by some applications.

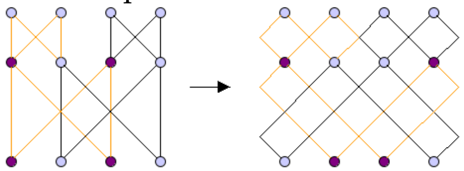
Wise Layout (6)



- CONs:
  - “slanted” lines, so that the area of the layout is measured by a rectangle whose sides are not parallel to coordinate axes but lie at 45°; if we follow the standard definition of layout area, it becomes $2(N-1) \times 2(N-1)= 4N^2+o(N^2)$; indeed, the circumscribed square with sides parallel to the coordinate axes has side equal to to the length of the path from the upper-left node to the lower-right node, that is $2(N-1)$;
  - …

Wise Layout (7)

- CONs (cntd.):
  - … it is a ‘cheating’ layout, indeed the “knock-knees” are not avoided but arranged in the layout thanks to some devices that have no null area and so enlarge the layout area.
  - The Wise layout “looks like” the usual representation. Nevertheless, in order to get the Wise layout from the usual representation, nodes must be permuted:

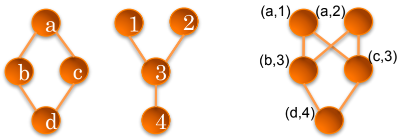


Even and Even Layout (1)

- This layout has been presented by G.Even and S.Even [’00], and it is based on the notion of Layered Cross Product
- **Def.** A *layered graph of $l+1$ layers $G=(V_0, V_1, \ldots, V_l, E)$* consists of $l+1$ layers of nodes; V_i is the (non-empty) set of nodes in layer i; E is a set of directed edges: edge (u,v) connects two nodes of two adjacent layers, that is, if u lies on layer i then v lies on layer $i+1$.

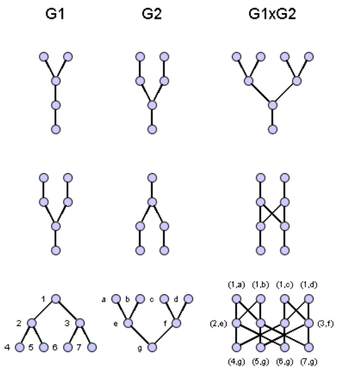
Even and Even Layout (2)

- **Def.** [Even & Litman ’92] The *Layered Cross Product (LCP)* of two layered graphs of $l+1$ layers each, $G^1=(V_0^1, V_1^1, \ldots, V_l^1, E^1)$ and $G^2=(V_0^2, V_1^2, \ldots, V_l^2, E^2)$, is a layered graph of $l+1$ layers, $G=(V_0, V_1, \ldots, V_l, E)$, where:
  - For every $i=0, \ldots, l$, $V_i = V_i^1 \times V_i^2$ (i.e. each layer is the cartesian product of the corresponding layers in G^1 and G^2);
  - There is an edge (u,v) in G connecting nodes (u^1,u^2) and (v^1,v^2) iff (u^1,v^1) and (u^2,v^2) are edges in G^1 and G^2, respectively.



Even and Even Layout (3)

Exemples of LCP



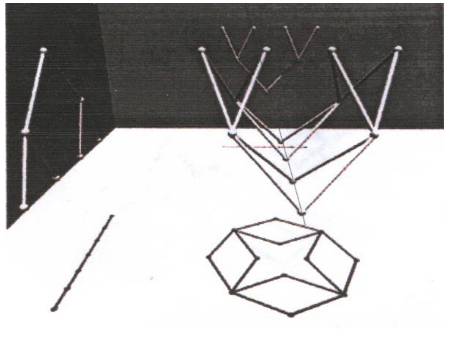
Even and Litman proved that many well known topologies are the LCP of simple structures (e.g. trees).

Namely, the butterfly network is the LCP of two binary trees, one of them is upward and the other one is downward.

Even and Even Layout (4)

The Projection Methodology (PM):

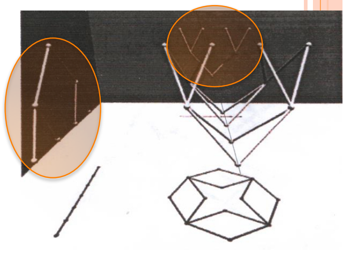
- Let G^1 and G^2 two layered graphs of $l+1$ layers each and let G denote their LCP. A layout of G is obtained with the PM as follows:



Even and Even Layout (5)

The Projection Methodology (contd.):

- Consider a cube and draw the graph G^1 on the xy face so that
  - (a) the y-coordinate of every node u e V_i^1 equals i
  - (b) the x-coordinate of every node is an integer.
- Similarly, draw the graph G^2 on the yz face
- …

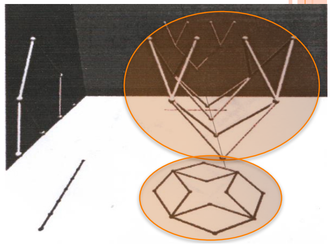


Even and Even Layout (6)

The Projection Methodology (cntd.):

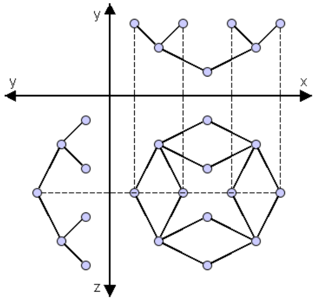
- … A three-dimensional drawing of the LCP G is constructed in the cube as follows:
  - if $u \in V_i^1$ is drawn in coordinates $(x_u, i, 0)$ and $v \in V_i^2$ is drawn in coordinates $(0, i, z_v)$, then the coordinates of node $(u,v) \in V_i$ are (x_u, i, z_v).

    In other words, the nodes of G are the intersections between the lines orthogonal to plane xy and passing through nodes of G^1 and the lines orthogonal to plane yz and passing through nodes of G^2.
- A 2D drawing of G is obtained by projecting the 3D drawing to the xz plane.

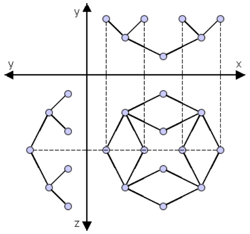


Even and Even Layout (7)

Obs. It is possible to avoid to construct the 3D representation by immediately using the prolongations on plane xz of the projections of nodes in layer i of G^1 on the x axis and of node in layer i of G^2 on the z axis, $i=0,\dots,l$



EVEN AND EVEN LAYOUT (8)

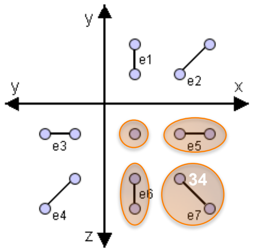


- The PM may produce layouts that do not satisfy the constraints required by the Thompson model.
  - For example, the drawing above is a grid drawing but it is not an orthogonal drawing.
- We now describe how rectilinear layouts of *G* can be obtained via the PM. First, we formalize necessary and sufficient conditions:
  - for the edges of the *xz* projection of *G* to be along grid paths,
  - for nodes to be mapped to different grid points, and
  - for not using any grid edge more than once.

EVEN AND EVEN LAYOUT (9)

Four types of edges in the product graph *G*:

1. The product of two diagonal edges yields a diagonal edge;
2. The product of a vertical edge and a diagonal edge yields a vertical edge;
3. The product of a diagonal edge and a vertical edge yields a horizontal edge;
4. The product of two vertical edges yelds a single grid point.



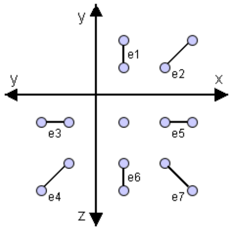
EVEN AND EVEN LAYOUT (10)

- In order to get a feasible layout through the PM, we have to impose that the product of either two diagonal edges or two vertical edges never occurs.

  More precisely:
- *1. The PM generates a layout of G in which the edges are grid lines if and only if the drawings of G^1 and G^2 on the faces of the cube satisfy the following condition: For every edge e e E, exactly one of its factor is drawn diagonally.*
- This claim avoids overlappings of nodes of the same layer, too.

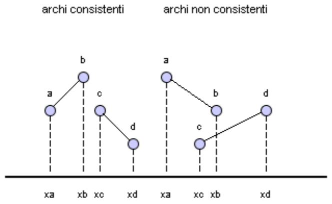
EVEN AND EVEN LAYOUT (11)

- We need to impose that nodes in different layers do not overlap:
- *2. The PM generates a layout of G in which at most one node is mapped to each grid point if and only if the sets$\{(x_u, z_v)$: $u \in V_i^1$ e $v \in V_i^2\}$ are disjoint, for each i=0, …, l.*
-



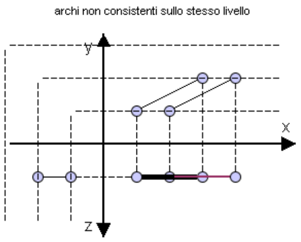
Even and Even Layout (12)

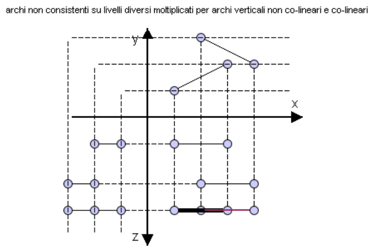
- Consider now two diagonal edges *(a,b)* and *(c,d)* in G^1; the coordinates of nodes *a, b, c, d* are:
  - node *a*: $(x_a, i, 0)$;
  - node *b*: $(x_b, i+1, 0)$;
  - node *c*: $(x_c, j, 0)$;
  - node *d*: $(x_d, j+1, 0)$.
- We say that these two edges are *consistent* if the open intervals (x_a, x_b) and (x_c, x_d) are disjoint.



Even and Even Layout (13)

- ***3.*** *The PM generates a layout of G in which no grid edge is used twice if and only if for every two inconsistent edges of one of the multiplicands the following condition holds:*
  - *The two edges are not in the same layer of the multiplicand, and*
  - *on the two layers in which they appear, there are no (straight) edges of the other multiplicand which are collinear.*




archi non consistenti su livelli diversi moltiplicati per archi verticali non co-lineari e co-lineari
y
x
z

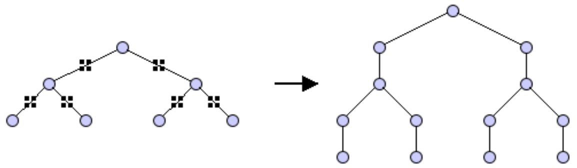
Even and Even Layout (14)

- In order to produce a feasible layout, we need to impose that all the three claims are satisfied.
- Let us consider the Claims one by one:

Even and Even Layout (15)

- ***1.*** *The PM generates a layout of G in which the edges are grid lines if and only if the drawings of G^1 and G^2 on the faces of the cube satisfy the following condition: For every edge e e E, exactly one of its factor is drawn diagonally.*
- A solution is to double the number of edge levels so that edges in the drawing of G^1 are diagonal in odd layers and straight in the even layers, while the edges in the drawing of G^2 are straight in the odd layers and diagonal in the even layers.

Even and Even Layout (16)



The doubling of the number of edge levels is achieved by stretching each edge of the two multiplicands to become a path of two edges.

In this way we simulate the creations of edge bends.

Even and Even Layout (17)

- *2. The PM generates a layout of G in which at most one node is mapped to each grid point if and only if the sets{(x_u, z_v): u ∈ V_i^1 e v ∈ V_i^2} are disjoint, for each i=0, …, l.*

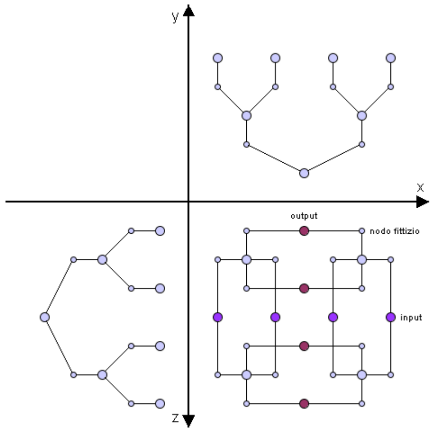
- A simple way to guarantee that this condition will hold is to make sure that no two nodes in the drawing of G^1 (G^2), except for the two end-points of the same straight edge, share the *x*-coordinate (*z*-coordinate).
- This is always possible if we opportunely enlarge the drawings of the two factors.

Even and Even Layout (18)

- *3. The PM generates a layout of G in which no grid edge is used twice if and only if for every two inconsistent edges of one of the multiplicands the following condition holds:*
  - *The two edges are not in the same layer of the multiplicand, and*
  - *on the two layers in which they appear, there are no (straight) edges of the other multiplicand which are collinear.*

- This condition is harder to enforce and is a severe limitation on this technique. For this reason, we limit to networks, each of which is the LCP of two trees.

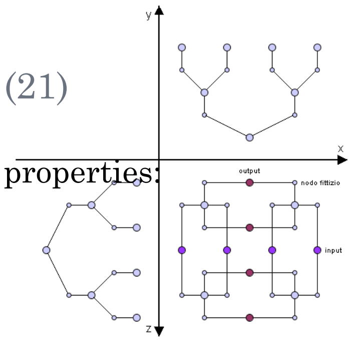
Even and Even Layout (19)



EVEN AND EVEN LAYOUT (20)

- The butterfly network is the LCP of two binary trees, one drawn upward and one drawn downward. (We dedicate a column to each vertex to prevent vertices of the layout from colliding.)
- Proceed as follows:
  - Draw one tree next to the *xy* plane and the other next to the *yz* plane
  - Construct their LCP in 3D inside the cube, in such a way that the two trees are the projections of the resulting butterfly on the *xy* and *yz* planes
  - The projection of this 3D figure on the floor is a planar layout of the butterfly

EVEN AND EVEN LAYOUT (21)



- This layout has the following properties:
  - It's symmetric;
  - Its height is $H=2(N-1)$;
  - Its width is $W=2(N-1)$;
  - Its area is $4N^2+o(N^2)$;
  - Input and output nodes are not on the boundary (negative property…)
  - All the edges on the same layer has the same length.

COMPARING THE TWO TECHNIQUES

- WISE - PROs:
  - relatively small area
  - It "looks like" a butterfly
  - Input/output nodes on the boundary
- WISE - CONs:
  - knok-knees
  - "slanted" grid
- EVEN & EVEN - PROs:
  - It eliminates all the flaws
- EVEN & EVEN - CONs:
  - Larger area
  - input/output nodes inside the layout

OTHER RESULTS (1)

- With the aim of optimizing the layout area, other layout algorithms have been proposed:
  - Dinitz ['98] proves that the area of the Even & Even layout can me decreased by means of some local adjustments, so to achieve area $11/6\ N^2+o(N^2)$
  - Later, Avior et al. ['98] prove that any butterfly layout cannot have area smaller than $N^2 + o(N^2)$ if "slanted" drawing is not allowed, and they provide an algorithm producing a layout of optimal area.

Other Results (2)

- Finally, Dinitz et al. ['99] prove that, if a "slanted" drawing is allowed, area $1/2\ N^2+o(N^2)$ is necessary and sufficient.

- These works definitively close the optimal area layout problem of the Butterfly network.

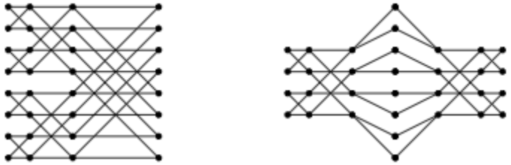
Optimal Area Layout of the Butterfly Network

Optimal Area Layout- Idea (1)

- The two papers that provide an optimal area layout base their result on the following lemma:

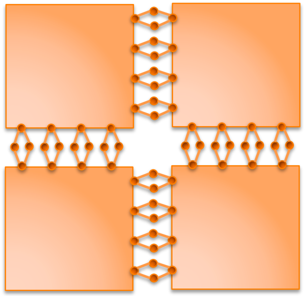
Lemma: For any nonnegative integers j, k, $0 \leq j \leq j+k \leq n$, the subgraph of the n-dim. Butterfly induced by the nodes of levels $j, j+1, \ldots, j+k$ is the disjoint union of 2^{n-k} copies of k-dimensional butterflies.

- In particular,if $j=0$ and $k=n-1$:



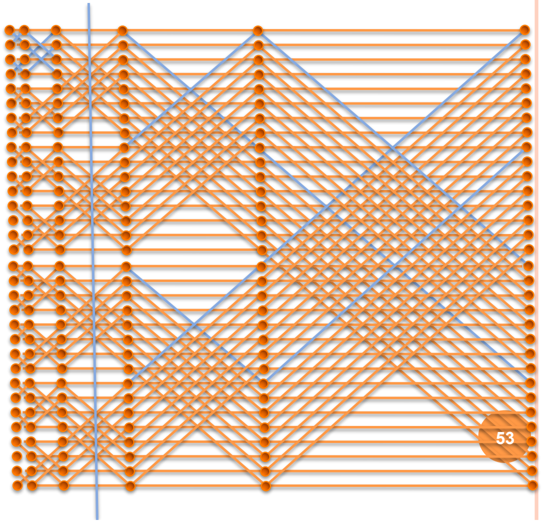
Optimal Area Layout- Idea (2)

- Hence, an $(n-1)$-dimensional Butterfly can be built as a pair of $(n-2)$-dim. Butterflies connected by one node layer and one edge layer.
- If we cut out the input and output nodes from an n-dim. Butterfly, we get:



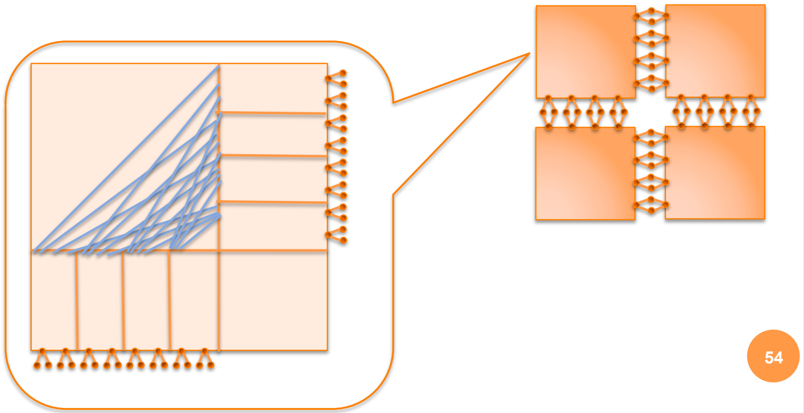
Optimal Area Layout- Idea (3)

- Each one of these *(n-2)*-dim. Butterflies can be, in turn, cut into many smaller butterflies:



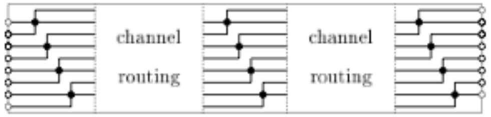
Optimal Area Layout- Idea (4)

- The previous layout can be better specified as follows:



Optimal Area Layout- Idea (5)

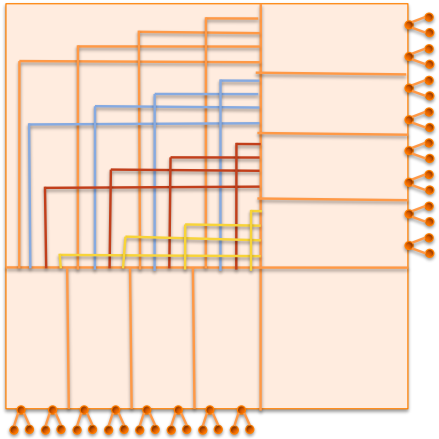
- Each rectangle contains a Butterfly that can be represented, either horizontally or vertically, layer by layer as follows:



- Obs.: this layout is far from being optimal; nevertheless it allows to produce a final optimal layout.

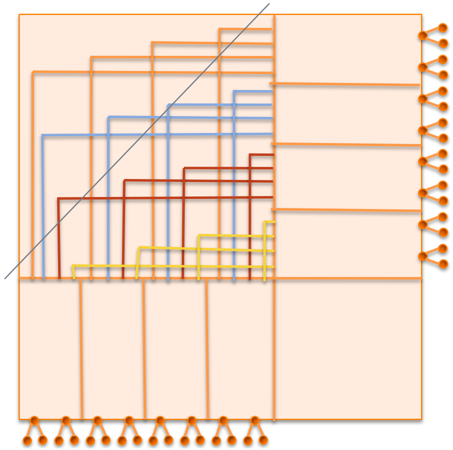
Optimal Area Layout - Idea (6)

- It remains to connect the small rectangular butterflies:



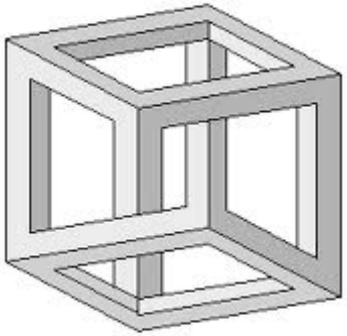
Optimal Area Layout - Idea (7)

- In the case of slanted layout, it can be bent along the line:



Optimal Area Layout - Idea (8)

- It is possible to prove tight lower and upper bounds on the layout area for both the models (usual and slanted).
- The interested students can look at:
  - A. Avior, T.C., S. Even, A. Litman, A.L. Rosenberg: A Tight Layout of the Butterfly Network. *Theory of Computing Systems* 31, 1998.
  - Y. Dinitz, S. Even, M. Zapolotsky: A Compact Layout of the Butterfly. *J. of Interconnection Networks* 4, 2003.

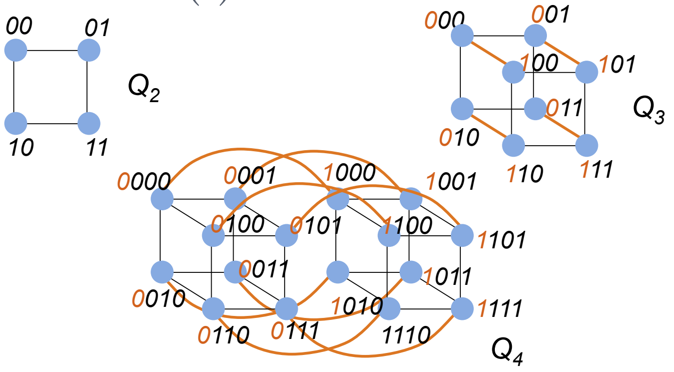


Layout of the Hypercube Network

The Hypercube (1)

- Widely used for parallel computation, thank to its nice properties (high regularity, logarithmic diameter, good fault tolerance, …).
- Def. The n-dimensional Hypercube, Q_n, has $N=2^n$ nodes and $n2^n$ edges. Each node is labeled with an n-bit binary string, and two nodes are linked with an edge iff their binary strings differ in precisely one bit.
- The edges of the hypercube can be naturally partitioned according to the dimensions that they traverse and Q_n: $Q_{n-1} \equiv Q_{n-1}$…

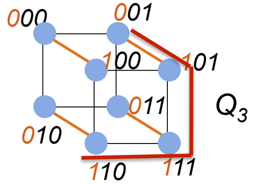
The Hypercube (2)



Q_n can be built by joining with an edge nodes in two different copies of Q_{n-1} if they have the same label.

Obs.: These edges form a perfect matching.

The Hypercube (3)



Property: Q_n has diameter *log N*.

Proof. Any two nodes $u=u_1u_2\ldots u_{logN}$ and $v=v_1v_2\ldots v_{logN}$ are connected by the path:

$u_1u_2\ldots u_{logN} \rightarrow v_1u_2\ldots u_{logN} \rightarrow v_1v_2\ldots u_{logN} \rightarrow \ldots \rightarrow v_1v_2\ldots v_{logN}$

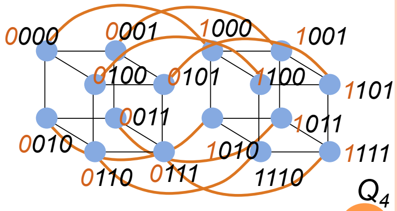
The claim trivially follows. CVD

The Hypercube (4)

Def. : The bisection width of a network is the minimum number of edges one has to cut to disconnect the network into two equally sized subnetworks.

Property. $BW(Q_n)=N/2$.

Proof. (idea) the red edges (=edges in a single dimension) divide the hypercube intwo two equally sized subnetworks; they are $N/2$ and it is not possible to cut a smaller number of edges to get the same result.



The Hypercube (5)

Th. A lower bound on the layout area of a network is the square of its bisection width.

Cor. Each layout of Q_n has area at least $N^2/4$.

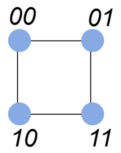
In the following: layout with area $4/9N^2+o(N^2)$, that hence is almost optimal (far from the lower bound by a factor of 1.7) [Yeh, Varvarigos, Parhami, '99].

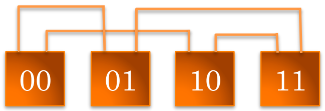
Again on the Thompson Model

- The Thompson model [Thompson '79] requires that the wires coming out of each processing elements are at most 4 (6 in 3D)
- What if the degree is higher? (end of the '90s)
  - A node of degree d occupies the area of a square of side d
  - The wires can run either horizontally or vertically along grid lines.

Collinear Layout (1)

- In a collinear layout all nodes are placed on the same line. Instead of computing its area, it is usual to count the number of necessary tracks.
- We start with a 2-dim. Hypercube, and inductively move to hypercubes of higher dimensions:
  - Q_2:

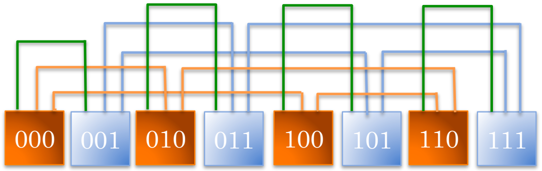




2 tracks

Collinear Layout (2)

- Assume that we have a collinear layout for Q_n that requires $f(n)$ tracks, where n is even: Q_{n+1}

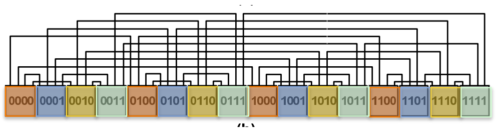


2 tracks 2 tracks 1 track

Tot. $f(n+1)=2f(n)+1$ track

Collinear Layout (3)

- To obtain the collinear layout of Q_{n+2} we start with the layouts of four Q_ns:



$f(n+2)=4f(n)+2$

Collinear Layout (4)

- Th. The number of tracks required for the collinear layout of Q_n is $2/3N$ (where $N=2^n$ is the number of nodes).
- Proof. We solve the following recurrence equation:
  - $f(n)=2f(n-1)+1$ if n odd
  - $f(n)=4f(n-2)+2$ if n even
  - $f(2)=2$

Even case:

$$f(n)=4f(n-2)+2=4^2f(n-4)+4\text{x}2+2=$$

$$=4^3f(n-6)+2^5+2^3+2=\ldots=4^k f(n-2k)+\sum_{i=0}^{k-1}2\cdot 4^i=$$

$=\ldots$when $n-2k=2$ iff $k=(n-2)/2\ldots=$

$$=4^{\frac{n-2}{2}}f(2)+2\sum_{i=0}^{\frac{n-2}{2}-1}4^i=2\sum_{i=0}^{\frac{n-2}{2}}4^i\cong 2\cdot\frac{4^{\frac{n-2}{2}+1}}{3}=\frac{2}{3}2^n=\frac{2}{3}N$$

Collinear Layout (5)

(proof cntd.)

The odd case is analogous. CVD

The area of this layout is $(2/3N+n)$ x (nN).

Th. Q_n can be laid out in $4/9N^2+o(N^2)$ area.

Proof idea. Let $n=n_1+n_2$.

Let us use 2^{n1} copies of the collinear layout of Q_{n2}, each placed along a row.

We connect the 2^{n1} nodes that belong to the same column vertically according to the collinear layout of a Q_{n1}.

Collinear Layout (6)

(proof cntd.)

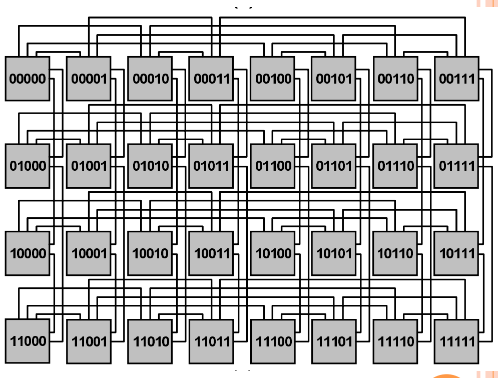
Reminder: Q_k needs of ${}_{2/3}n^k$ tracks

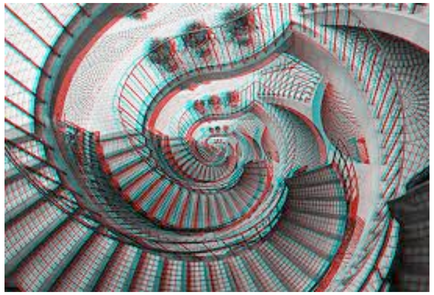
# of vertical tracks (rows) : 2^{n1} copies x ${}_{2/3}2^{n2}$ tracks

Additive height (nodes): 2^{n1} copies x n_2

The width is computed analogously, switching the roles of n_1 and n_2.

The claim follows choosing $n_1=\Theta(n_2)\cong n_{/2}$.

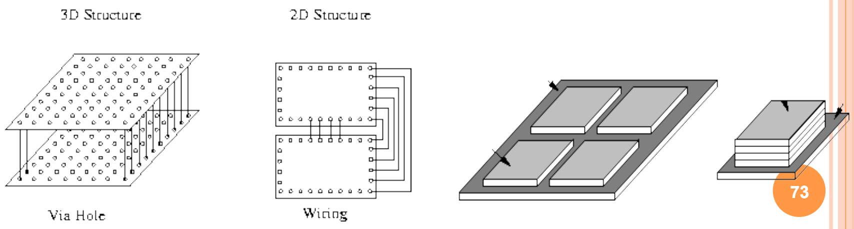




3D Layout

3D Layout Problem (1)

- The diffusion of the 3D layout has increased in the last thirty years.
- The topology is lain out on a series of slices.
- Further optimization of the wire length and number of bends
- Less silicon used.



The 3D Layout Problem (2)

Def. A 3D layout of a topology G is a 1-1 function between G and the 3D grid such that:

- the nodes are mapped into grid points
  - it is better if the nodes lie on the external slice in order to minimize: energy consuming, production of heat and difficulty of connection with other devices
- the wires are mapped on independent grid paths so that:
  - these paths are edge-disjoint;
  - there are no “knock-knees”
  - these paths do not cross any mapping of a node that is not an extreme of the corresponding wire.

Aim: minimizing the volume and keeping wires short.

The 3D Layout Problem (3)

The students interested in this topic can look at:

- L. Torok and I. Vrto. Layout Volumes of the Hypercube. *Proc. Graph Drawing ’04.*
- T.C. and A. Massini. Three Dimensional Layout of Hypercube Networks. *Networks* 47, 2006.