Advanced and parallel architectures

Prof. A. Massini

Mid Term Exam – April 14, 2015

Cognome Nome

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Exercise 1 (3 points)	
Exercise 2 (3 points)	
Exercise 3 (4 points)	
Exercise 4 (3 points)	
Exercise 5 (4 points)	
Exercise 6 (3 points)	
Exercise 7 (3 points)	
Question 1 (5 points)	
Question 2 (5 points)	
Total (33 points)	

Exercise 1 (3 points)

Consider the following loop expressed in a high level language:

for (i =0; i < N; i ++)
{
vectA[i] = vectB[i]
vectB[i] = vectB[i] + 4;
}

The program has been written in MIPS assembly code, assuming that registers $t6 and $t7 have been initialized with values 0 and 4N respectively. The symbol VECTB is a 16-bit constant.

Let us consider the loop executed by 5-stage pipelined MIPS processor WITHOUT any optimisation in the pipeline.

1. Identify the Hazard Type (Data Hazard or Control Hazard) in the last column

2. In the first column identify the number of stalls to be inserted before each instruction (or between stages IF and ID of each instruction) necessary to solve the hazards

3. For each hazard, add an ARROW to indicate the pipeline stages involved in the hazard

Num. Stalls	INSTRUCTION	C1	C2	C3	C4	C5	C7	C6	C8	C9	C10	C11	Hazard Type
	`FOR: beq $t6,$t7,END`	IF	ID	EX	ME	WB							
	`lw $t2,VECTB($t6)`		IF	ID	EX	ME	WB						
	`sw $t2,VECTA($t6)`			IF	ID	EX	ME	WB					
	`addi $t2,$t2,4`				IF	ID	EX	ME	WB				
	`sw $t2,VECTB($t6)`					IF	ID	EX	ME	WB			
	`addi $t6,$t6,4`						IF	ID	EX	ME	WB		
	`blt $t6,$t7, FOR`							IF	ID	EX	ME	WB	

Exercise 2 (3 points)

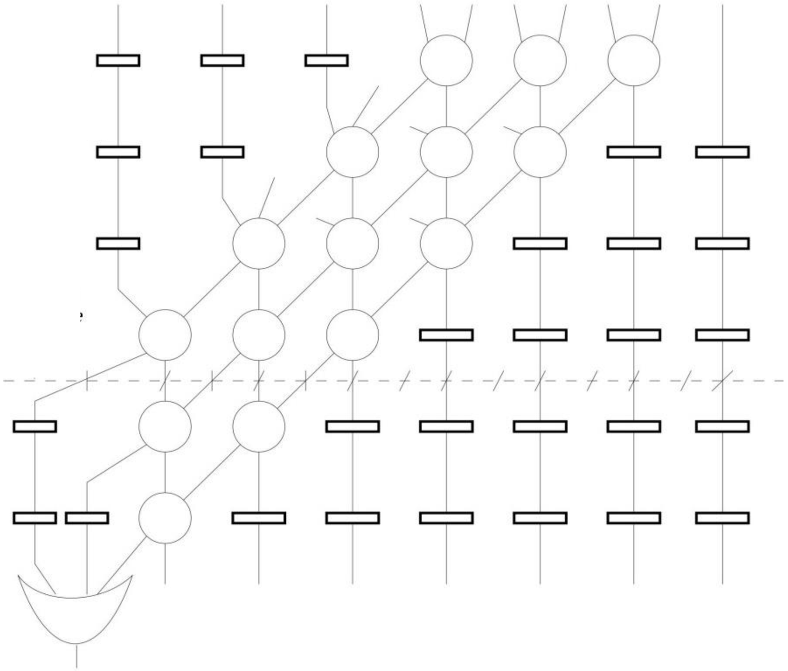
1. For each instruction, write the phases and insert the stalls to solve the hazards identified in Exercise 1. You should take into account that solving some hazards can help to solve those that follow

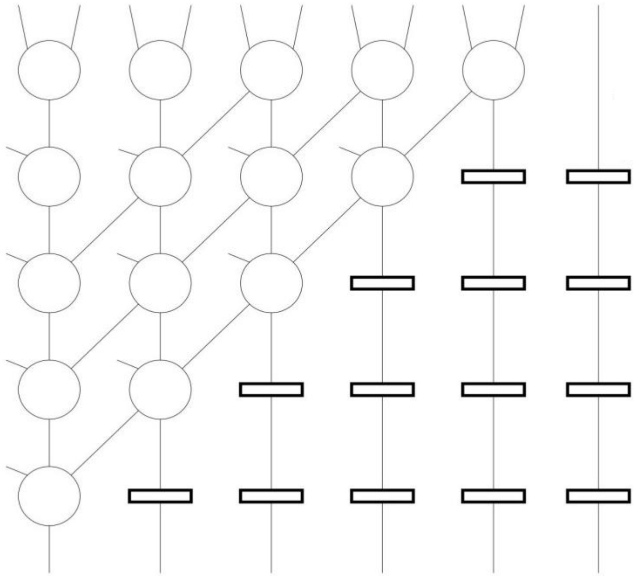
2. In the first column specify the number of stalls actually inserted

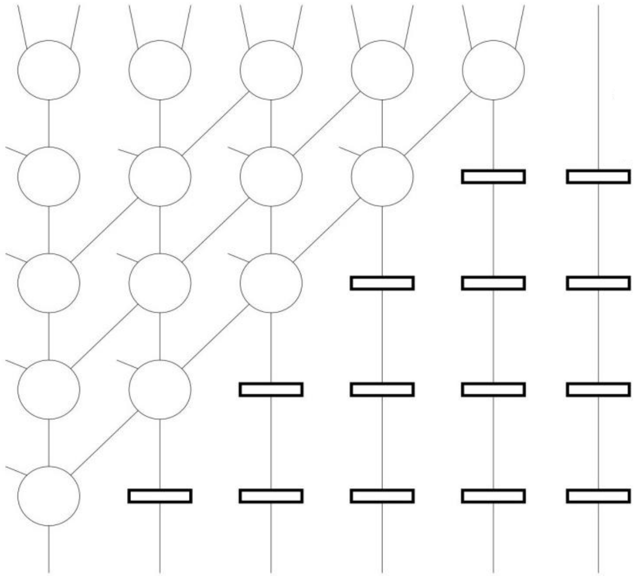
Num. Stalls	INSTRUCTION	C1	C2	C3	C4	C5	C7	C6	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24	C25
	`FOR: beq $t6,$t7,END`																									
	`lw $t2,VECTB($t6)`																									
	`sw $t2,VECTA($t6)`																									
	`addi $t2,$t2,4`																									
	`sw $t2,VECTB($t6)`																									
	`addi $t6,$t6,4`																									
	`blt $t6,$t7, FOR`																									

Exercise 3 (4 points)

Given the values A=3 and B=2, utilise the following schemes to obtain the result of the multiplications: AxB, Ax(-B) and (-A) x(- B). Verify the results.







Exercise 4 (3 points)

1. Given the value X= 00 01 11 10 expressed in the RB number system:
   - Give the correspondent value in the decimal system ____________________
   - Give at least three other expressions of X ____________________

2. Given the value Y= $\bar{1}011\bar{1}0$ expressed in the MSD number system:
   - Give the correspondent value in the decimal system ____________________
   - Give at least three other expressions of Y ____________________

Exercise 5 (4 points)

1. Modify the table below here used to execute the RB addition in such a way that the couple of bit in the upper row is 00 whenever it is possible.

	00	01	10	11
00	00 00	10 00	00 01	10 01
01	00 01	10 01	00 10	10 10
10	00 01	10 01	00 10	10 10
11	00 10	10 10	00 11	10 11

	00	01	10	11
00	00 00	00	00	
01				
10				
11				10 11

2. Show the execution of addition of A= 00 01 11 10 and B = 00 10 10 01 using both tables. Verify the value of the results.

- First operand - Second operand *- First table application* *- Second table application*	____________________ ____________________ ____________________ ____________________ ____________________ ____________________ ____________________
Result	____________________

- First operand - Second operand *- First table application* *- Second table application*	____________________ ____________________ ____________________ ____________________ ____________________ ____________________ ____________________
Result	____________________

Exercise 6 (3 points)

Draw the schemes of a **Carry ripple adder** and a **Pipelined adder** by using Half adders and Full adders as building blocks.

Exercise 7 (3 points)

Assume that the delay due to the propagation time of signals through a gate (*gate delay*) is τ_{gate}.

Also assume that the delay due to the propagation time through a FF D is equal to $2\tau_{gate}$.

1. What is the propagation time of a Half adder and a Full adder, using τ_{gate} as a parameter?

$\tau_{HA} =$ $\tau_{FA} =$

2. Calculate the speedup of the **pipelined adder** compared to a **Carry ripple adder** for the execution of h = 100 additions of *n* bit numbers, using τ_{gate} as a parameter.

Question 1 (5 points)

Explain what data hazards, control hazard and structural hazards are, when using instruction pipeline.

Question 2 (5 points)

Describe the classification of Flynn.