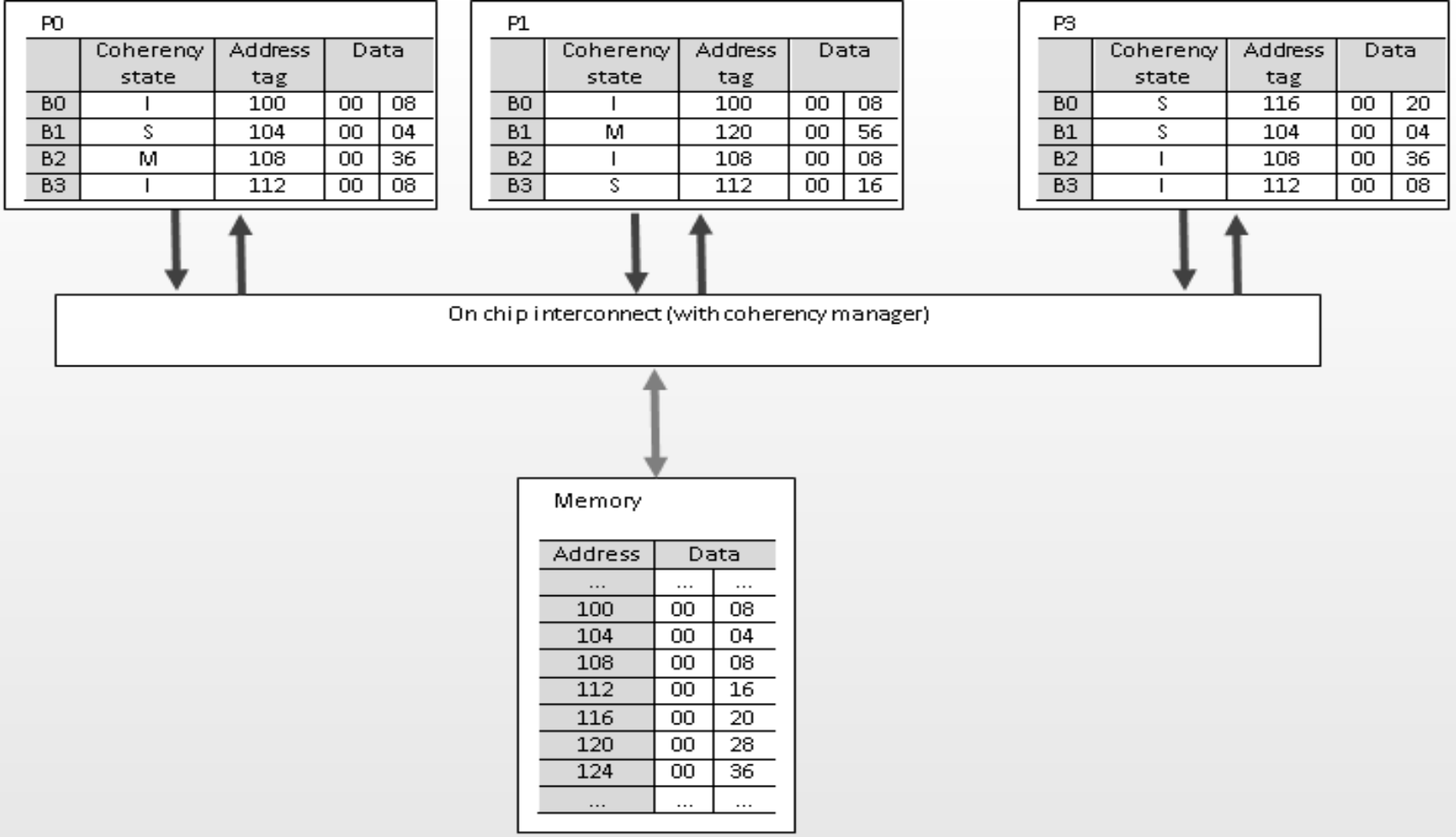
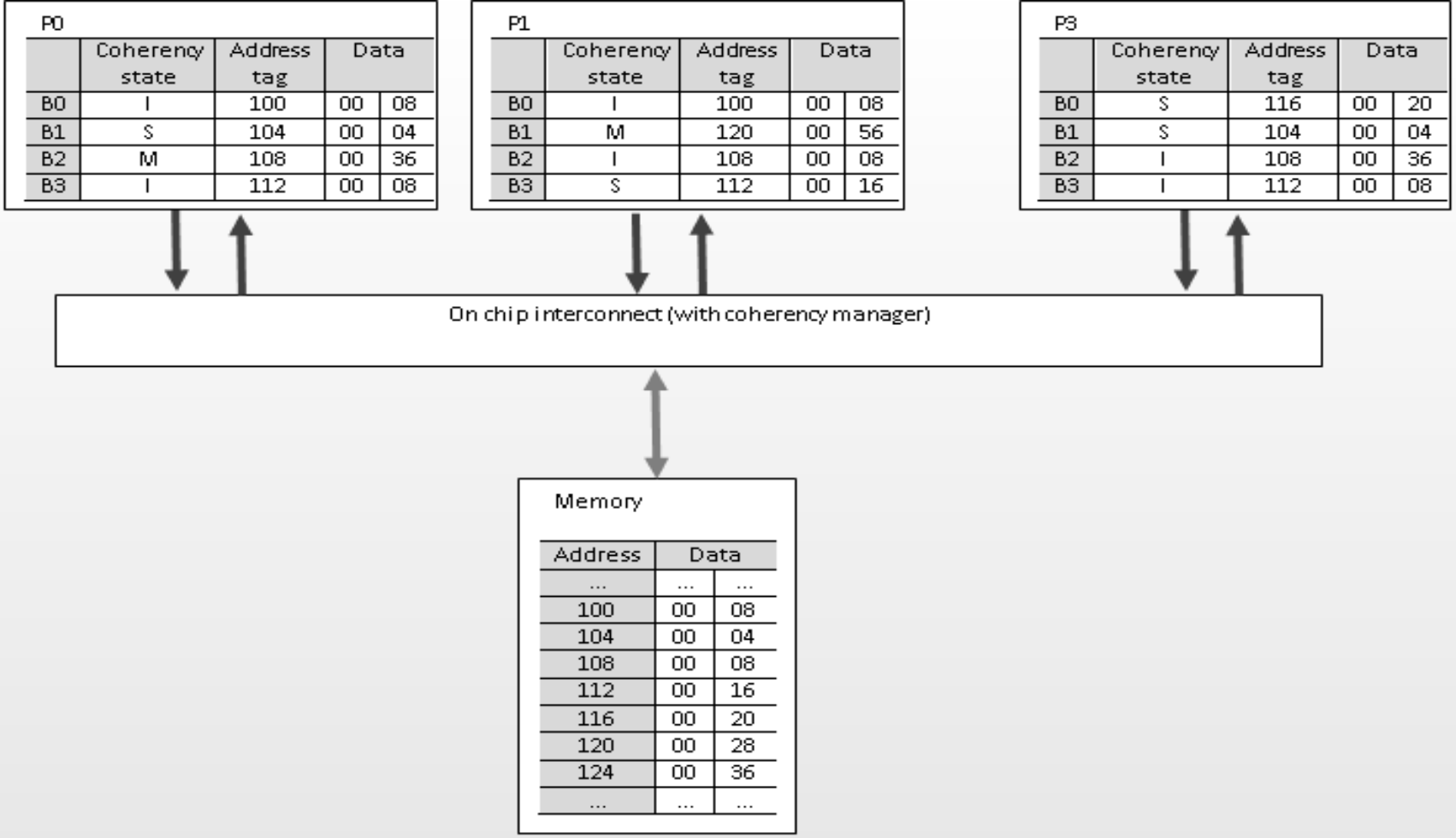
Advanced Parallel Architecture

Annalisa Massini - 2016/2017

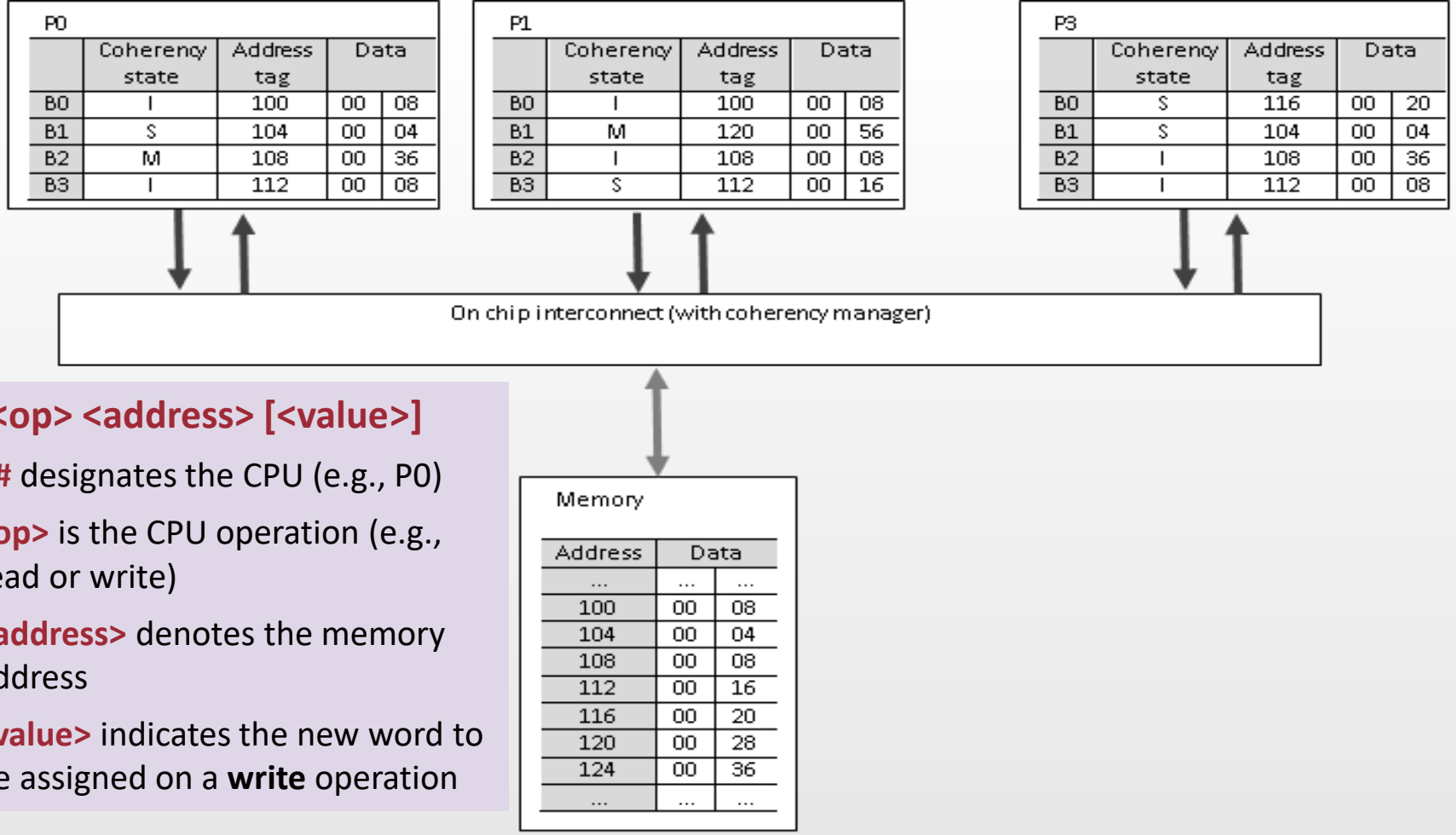
Cache Coherence: Exercises



- Consider a multicore multiprocessor implemented as a **symmetric shared-memory architecture**
- Each processor has a single, private cache
- Coherence is maintained using the **snooping coherence protocol**

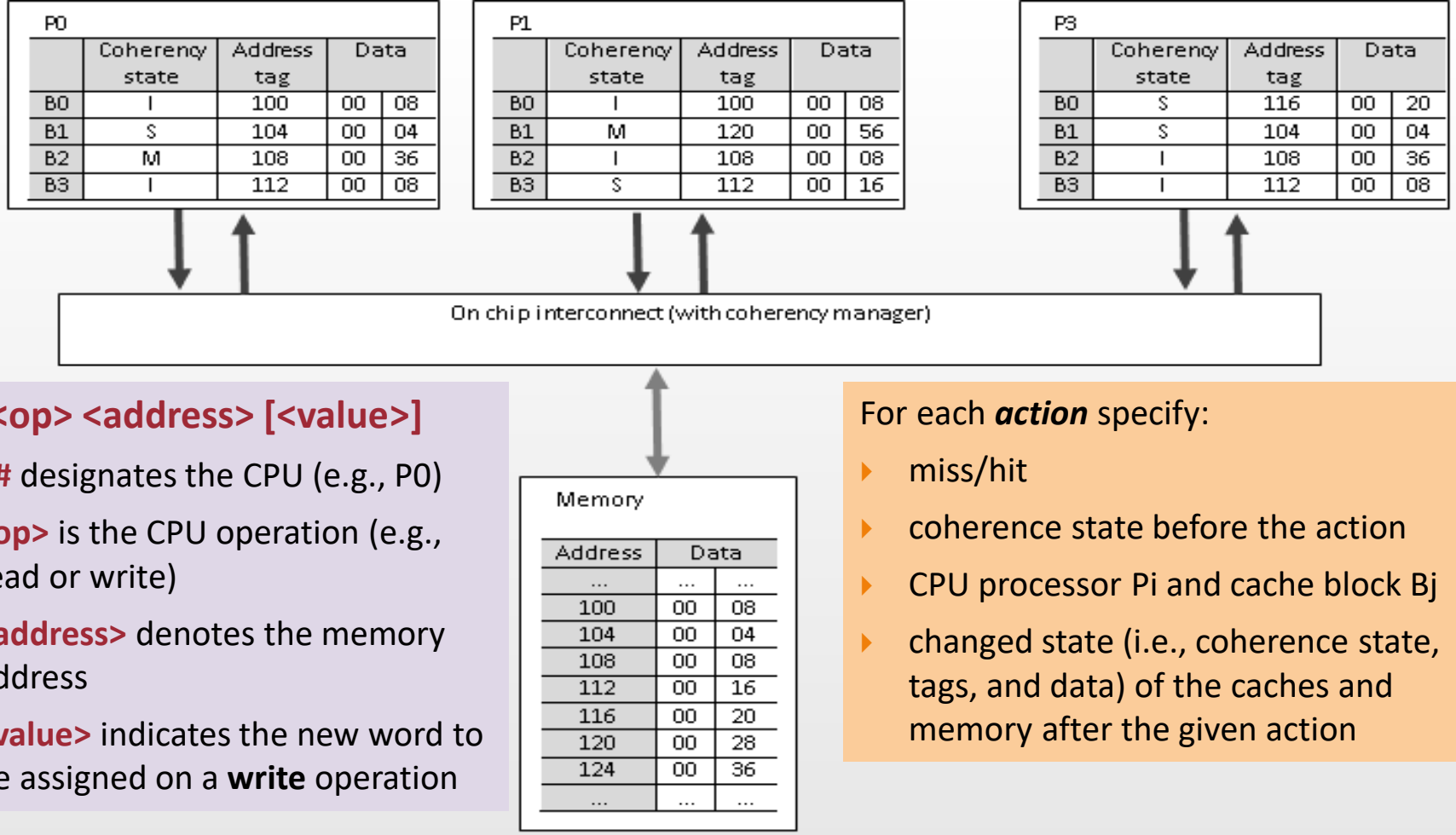


- Each cache is direct-mapped, with **four blocks** each holding **two words**
- The coherence **states** are denoted **M, S, and I** (Modified, Shared, and Invalid)



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

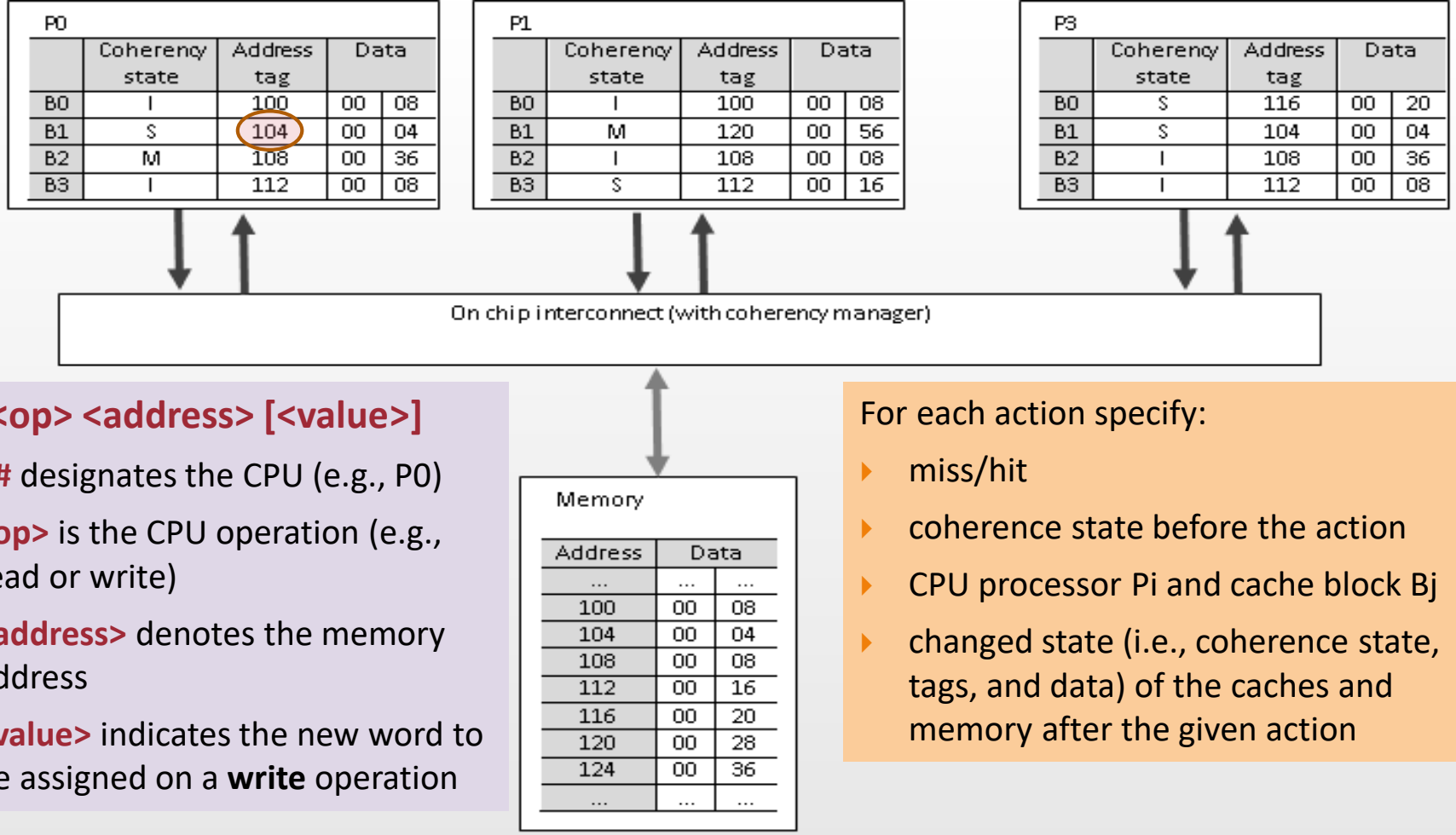


P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

For each ***action*** specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action



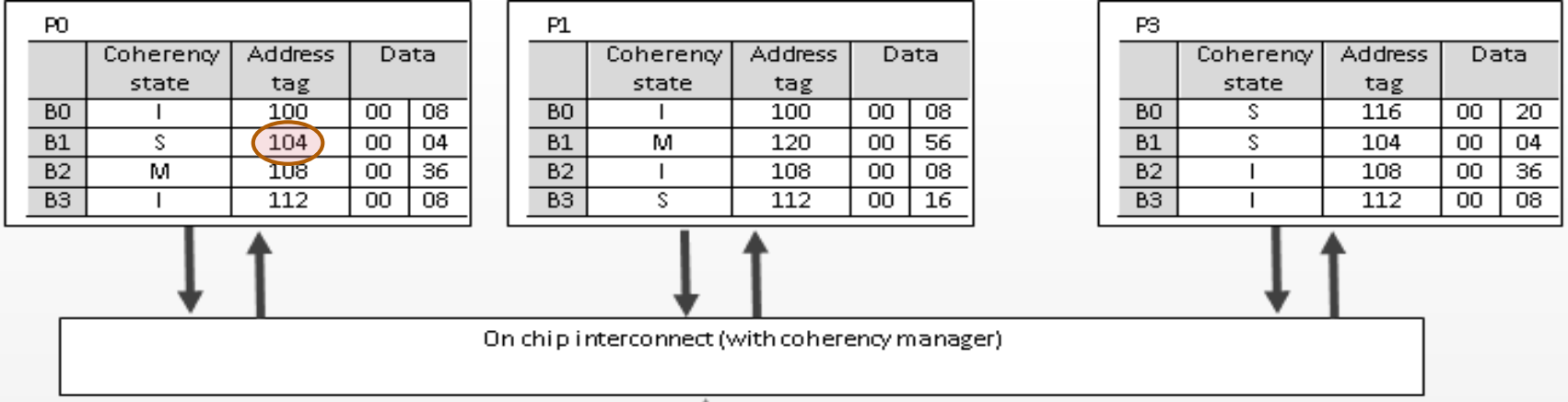
P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Exercise 5 - June 11th, 2015



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

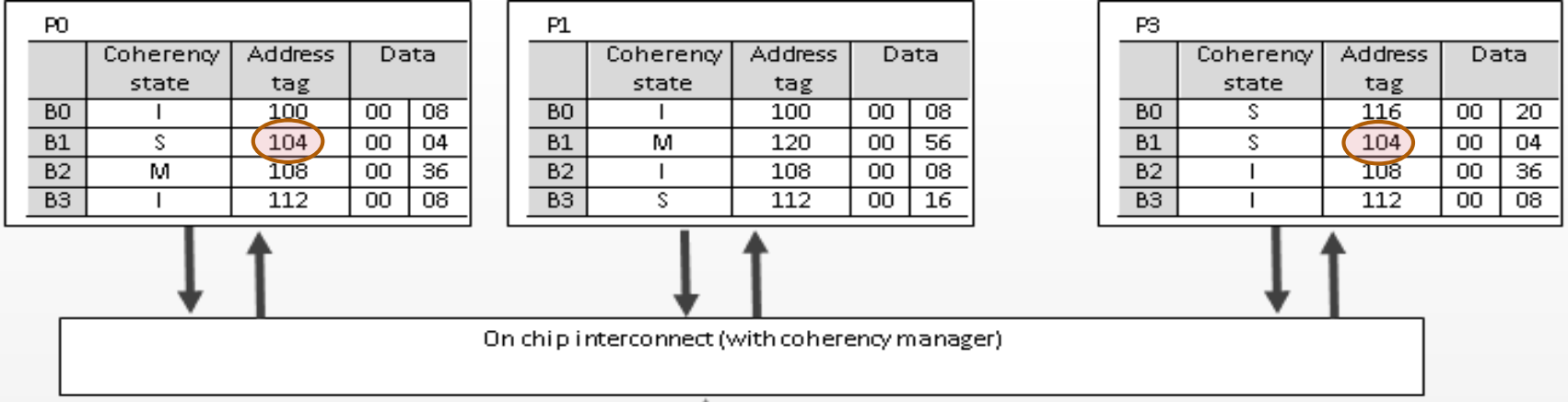
Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 104 ← 24**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

Memory

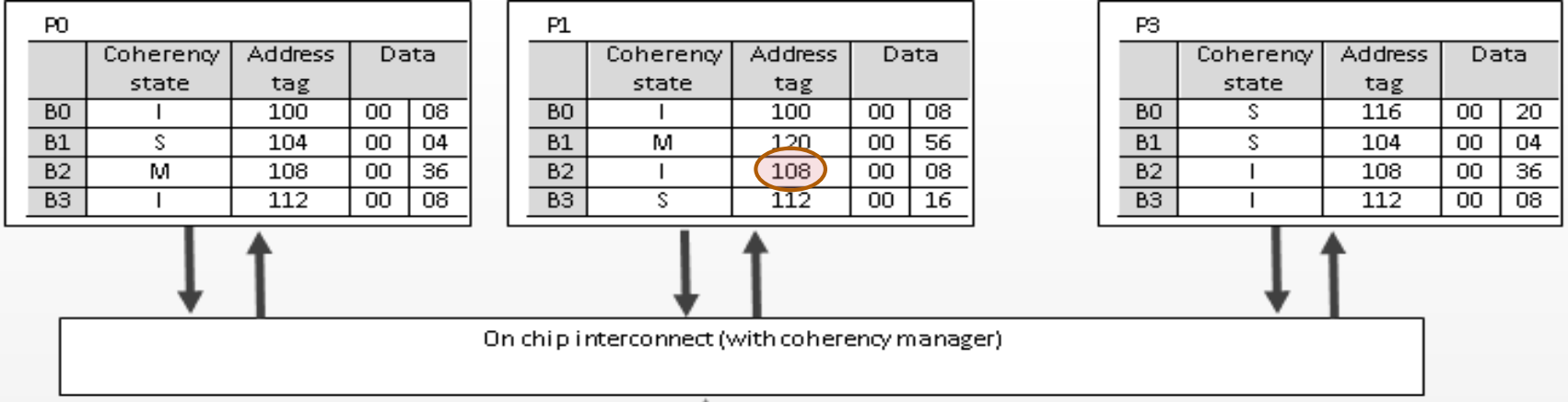
Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 104 ← 24**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
HIT	S	P0. B1 (M, 104, 00 24)
	S	P3. B1 (I, 104, 00 04)



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a **write** operation

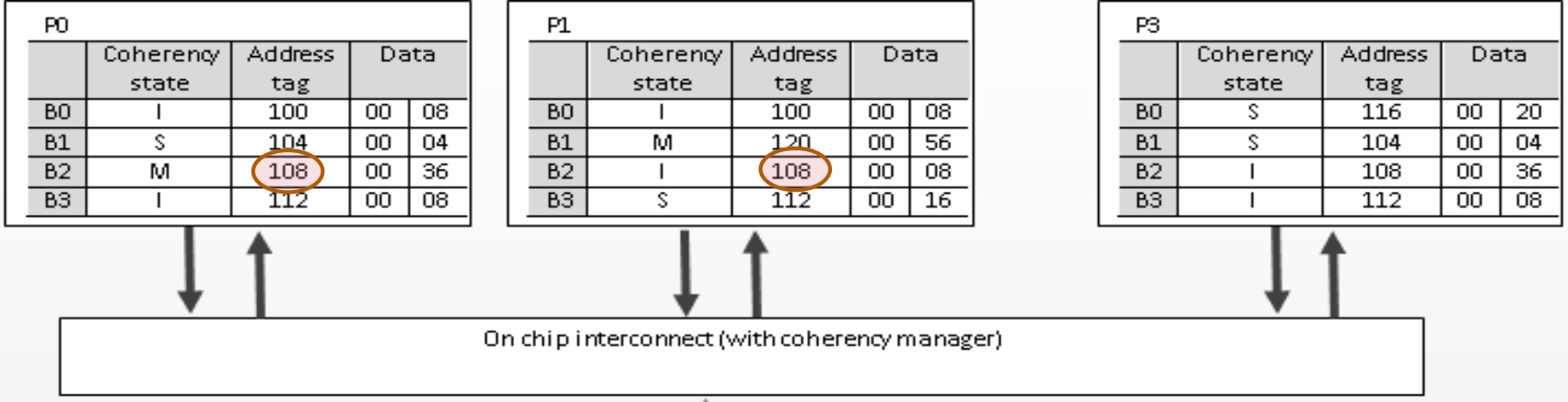
Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P1: read 108**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

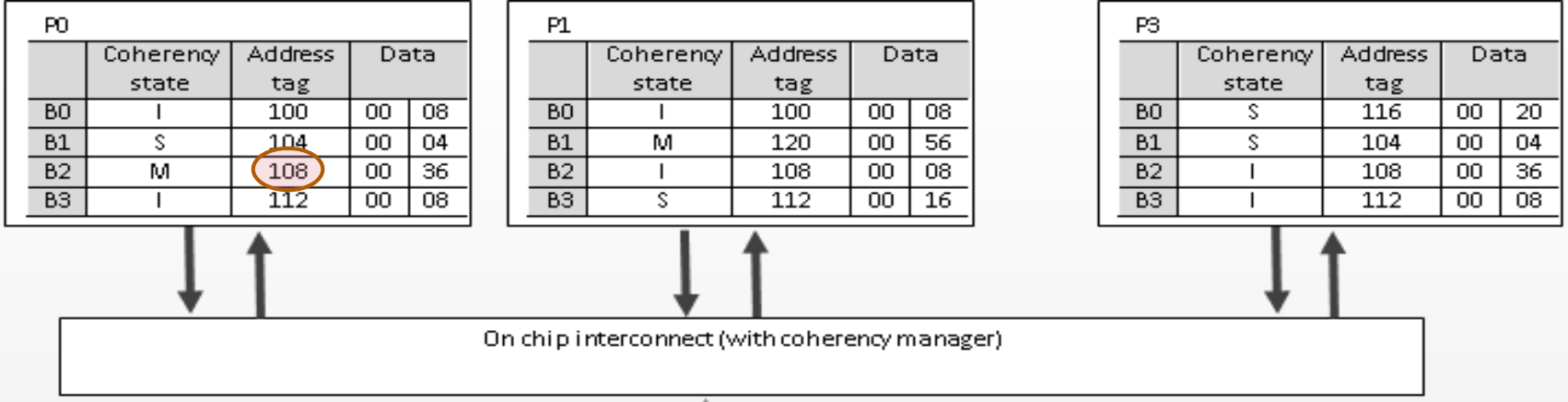
For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P1: read 108**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
MISS	I	P1. B2 (S, 108, 00 36)
	M	P0. B2 (S, 108, 00 36)

Returned value by read **00 36**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

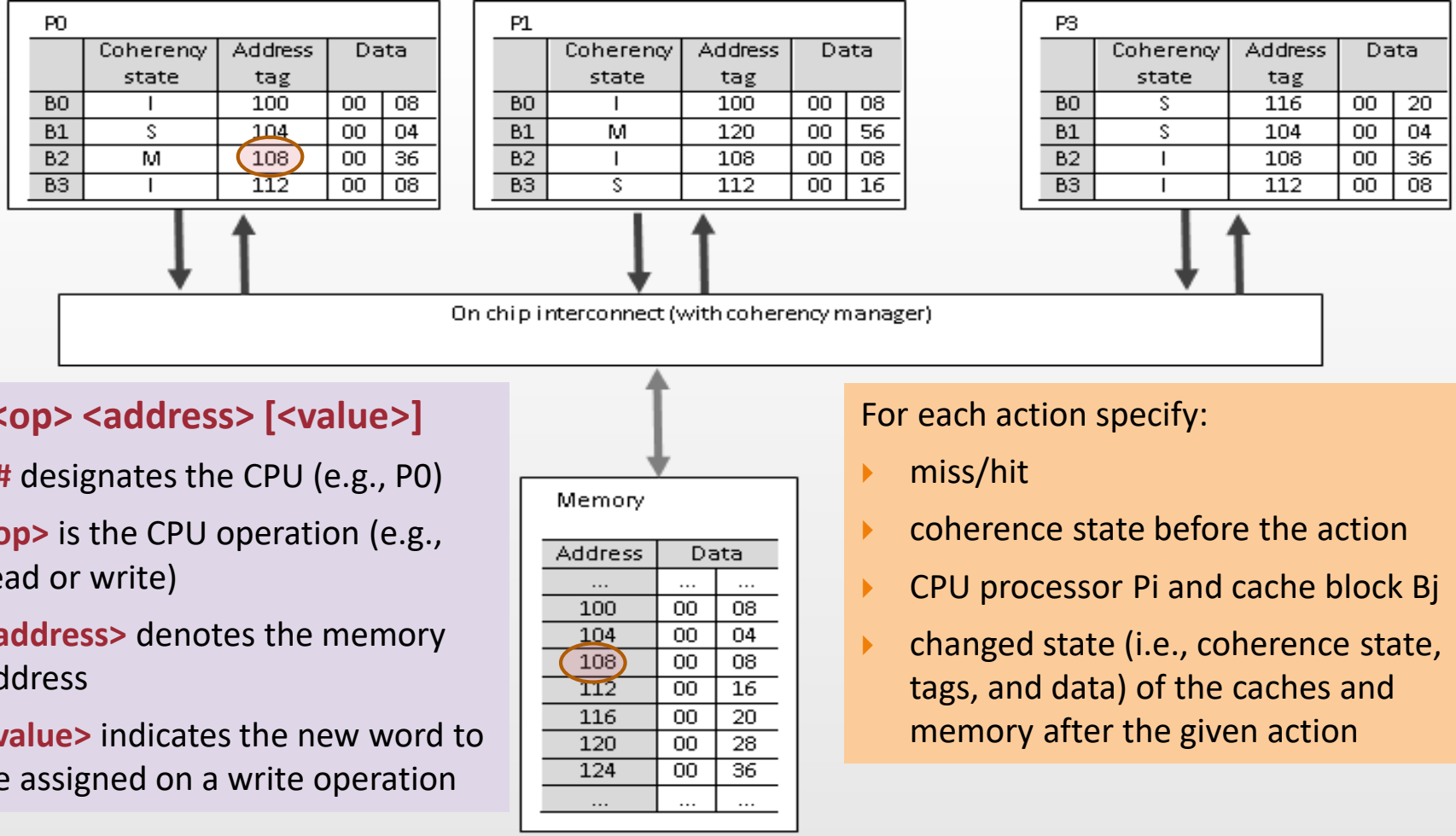
Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 124 ← 12**



P#: <op> <address> [<value>]

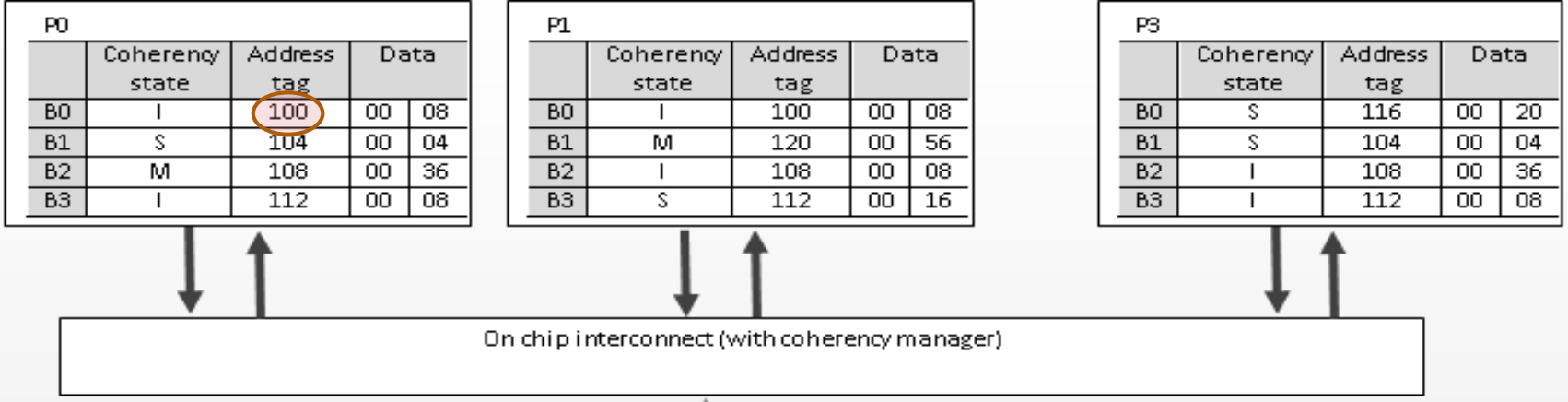
- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 124 ← 12**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
MISS	M	P0. B2 (M, 124, 00 12) *memory (108, 00 36)*



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

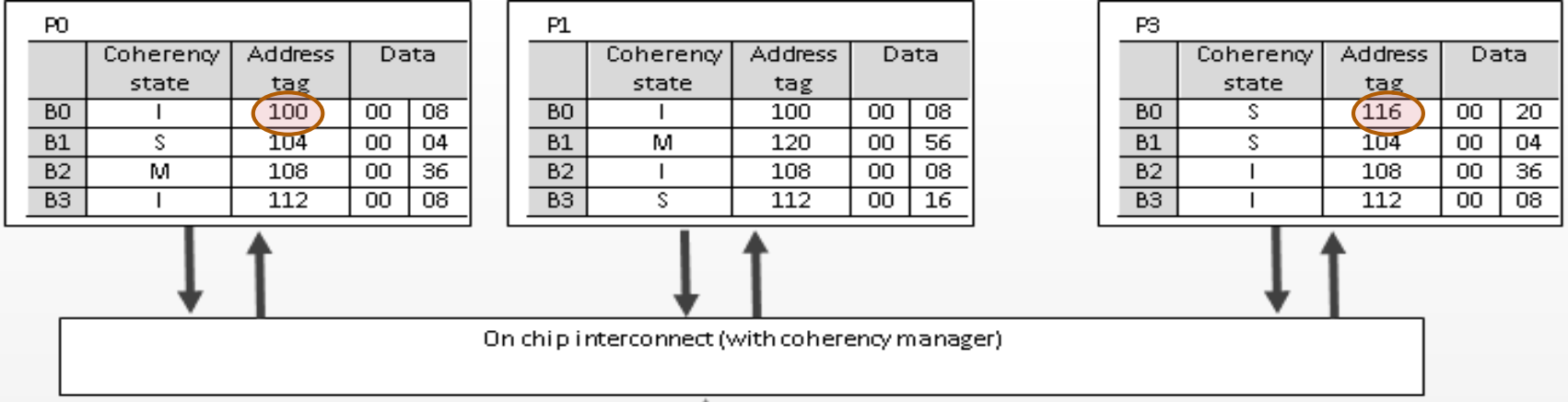
Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 116 ← 32**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

Memory

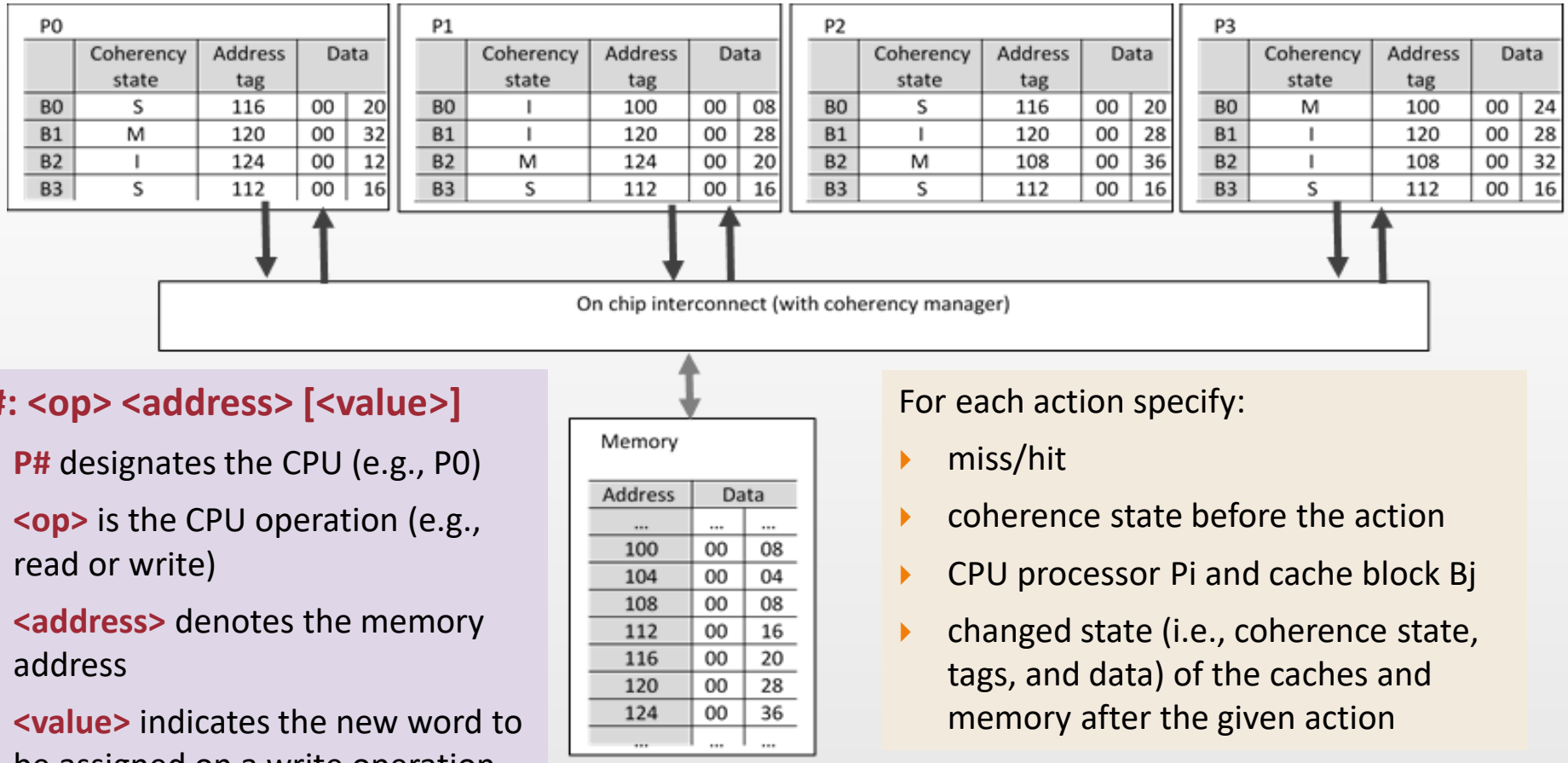
Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P0: write 116 ← 32**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
MISS	M	P0. B0 (M, 116, 00 32)
	S	P3. B0 (I, 116, 00 20)



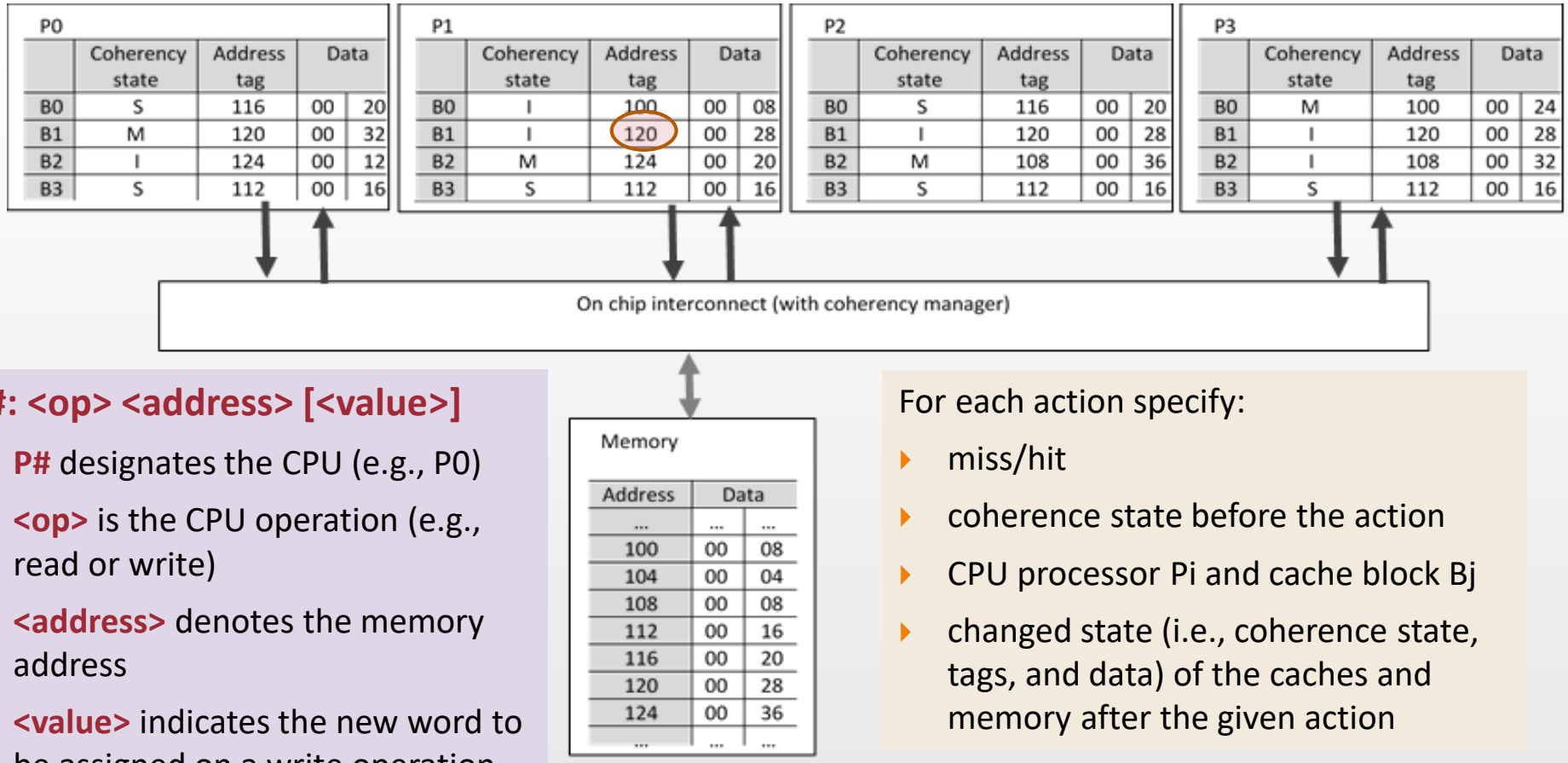
P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Exercise 4 - June 26th, 2015



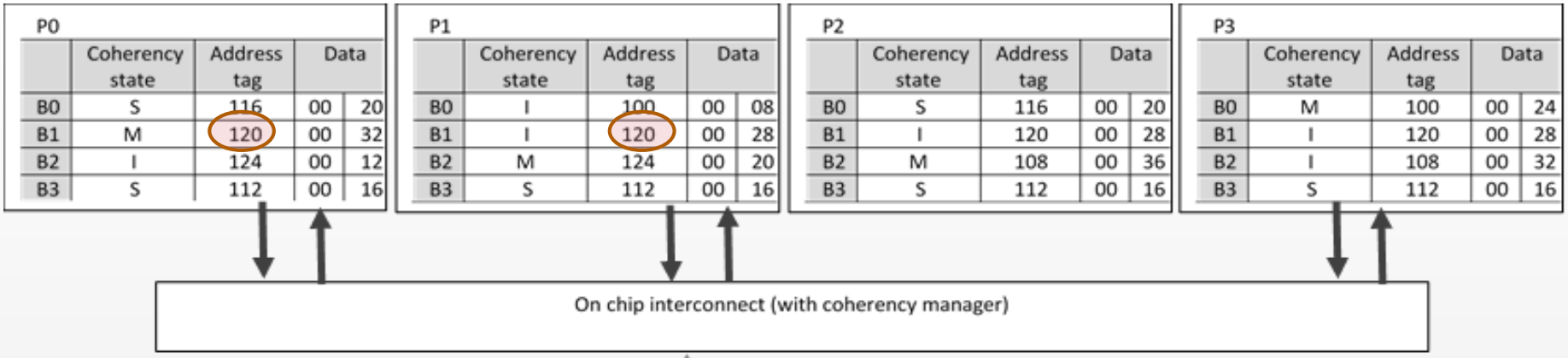
P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P1: write 120← 24**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

Memory

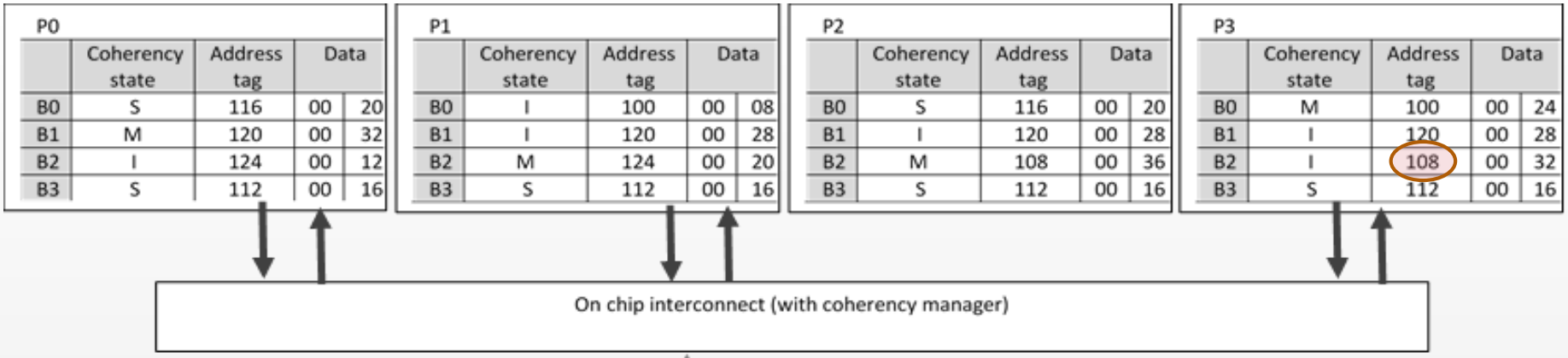
Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P1: write 120← 24**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
MISS	I	P1. B1 (M, 120, 00 24)
	M	P0. B1 (I, 120, 00 32)



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

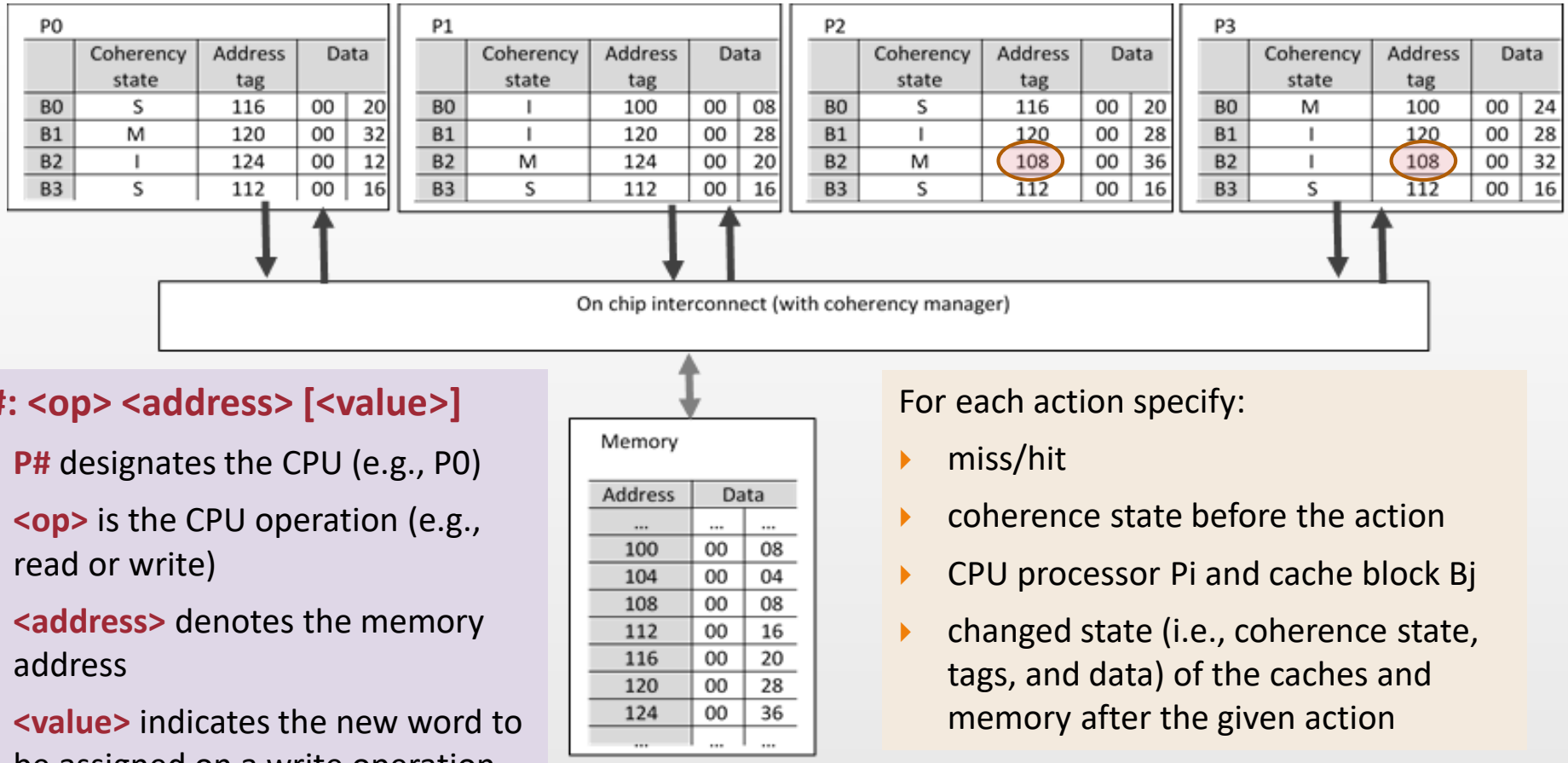
Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P3: read 108**



P#: <op> <address> [<value>]

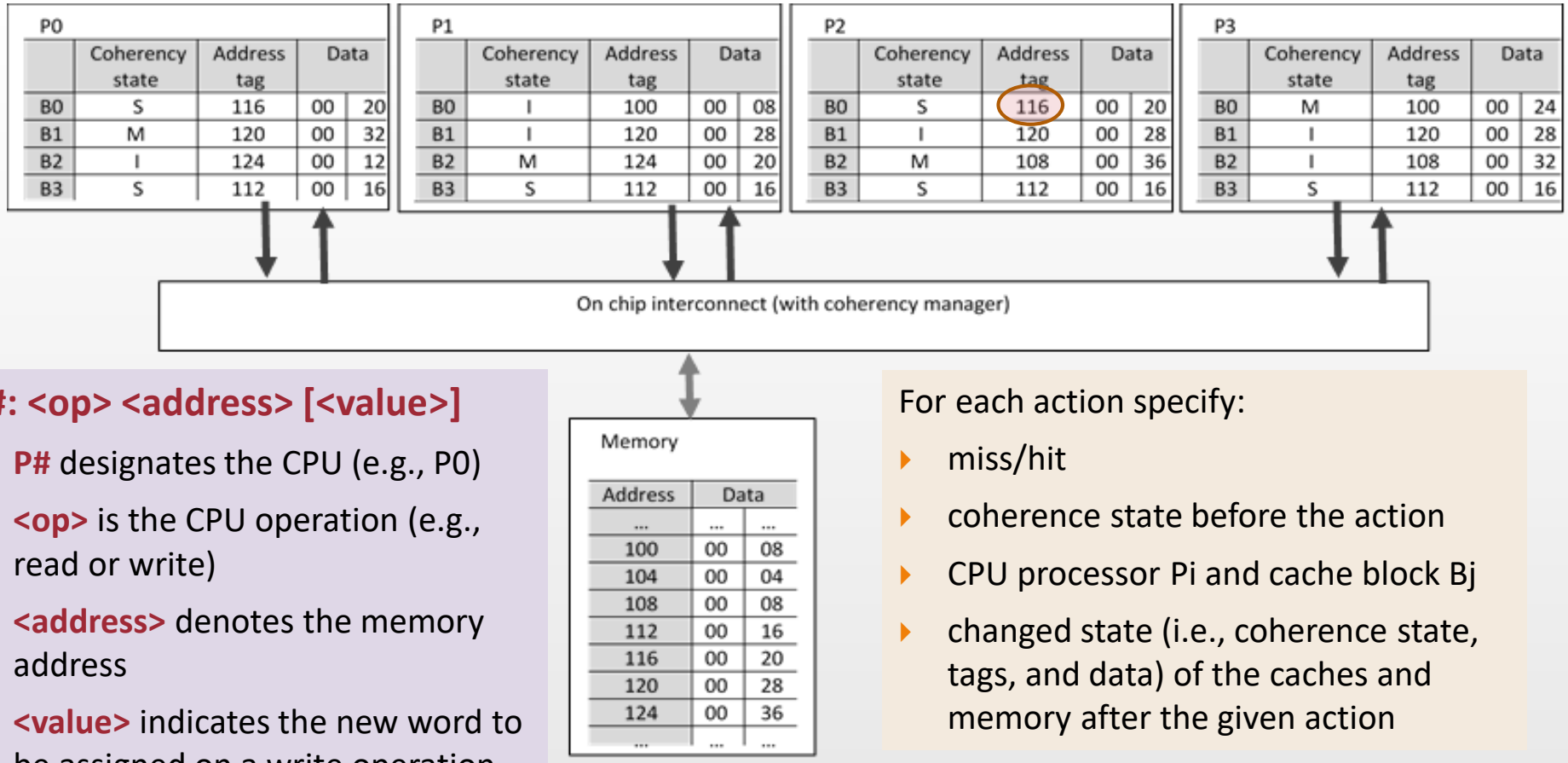
- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P3: read 108**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**	
MISS	I	P3. B2 (S, 108, 00 36)	***read 36***
	M	P2. B2 (S, 108, 00 36)	



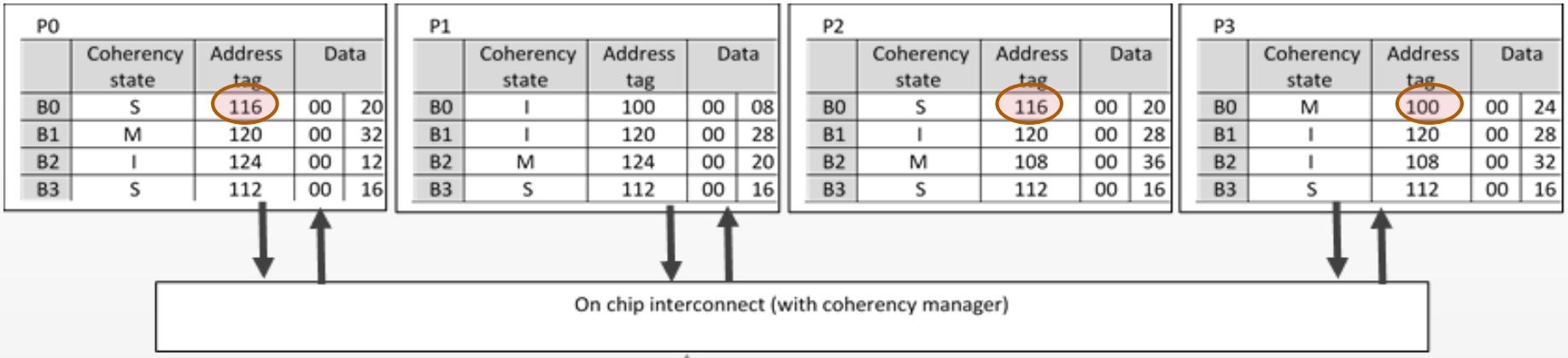
P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P2: write 100 ← 20**



P#: <op> <address> [<value>]

- **P#** designates the CPU (e.g., P0)
- **<op>** is the CPU operation (e.g., read or write)
- **<address>** denotes the memory address
- **<value>** indicates the new word to be assigned on a write operation

Memory

Address	Data	
...	...	...
100	00	08
104	00	04
108	00	08
112	00	16
116	00	20
120	00	28
124	00	36
...	...	...

For each action specify:

- miss/hit
- coherence state before the action
- CPU processor Pi and cache block Bj
- changed state (i.e., coherence state, tags, and data) of the caches and memory after the given action

Action **P2: write 100 ← 20**

hit/miss	**state before**	**Pi.Bj (state, tag, datawords)**
MISS	S	P2. B0 (M, 100, 00 20)
	S	P0. B0 (M, 116, 00 20)
	M	P3. B0 (I, 100, 00 24)