# Advanced Parallel Architecture

## Lesson 12

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# Exercise 1

- Compute Area $A_{CLA}$ and Time $T_{CLA}$ for the 4-bit carry-lookahead adder using the model for gate-count and gate-delay

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- Compute Area $A_{CLA}$ and Time $T_{CLA}$ for the 4-bit carry-lookahead adder using the model for gate-count and gate-delay

- Remember that:
  - **Any gate** (but the EX-OR) counts as **one gate** for both area and delay → $A_{gate}$ and $T_{gate}$
  - An **exclusive-OR gate** counts as **two elementary gates** for both area and delay → $A_{EX\text{-}OR} = 2A_{gate}$ and $T_{EX\text{-}OR} = 2T_{gate}$
  - An ***m*-input gate** counts as ***m* – 1 gates for area** and **$\log_2 m$ gates** for delay → $A_{m\text{-}gate} = (m-1)A_{gate}$ and $T_{m\text{-}gate} = \log_2 m \; T_{gate}$

# Carry-Lookahead Adder

- The carry-lookahead adder uses the bits:

  Carry Generate $g_i = a_i b_i$

  Carry propagate $p_i = a_i \oplus b_i$

  Then the expression of the carry is:

$$c_{i+1} = a_i b_i + (a_i \oplus b_i) c_i = g_i + p_i c_i$$

  And the expression of the sum is:

$$s_i = a_i \overline{b}_i \overline{c}_i + \overline{a}_i b_i \overline{c}_i + \overline{a}_i \overline{b}_i c_i + a_i b_i c_i = (a_i \oplus b_i) \oplus c_i = p_i \oplus c_i$$

# Carry-Lookahead Adder

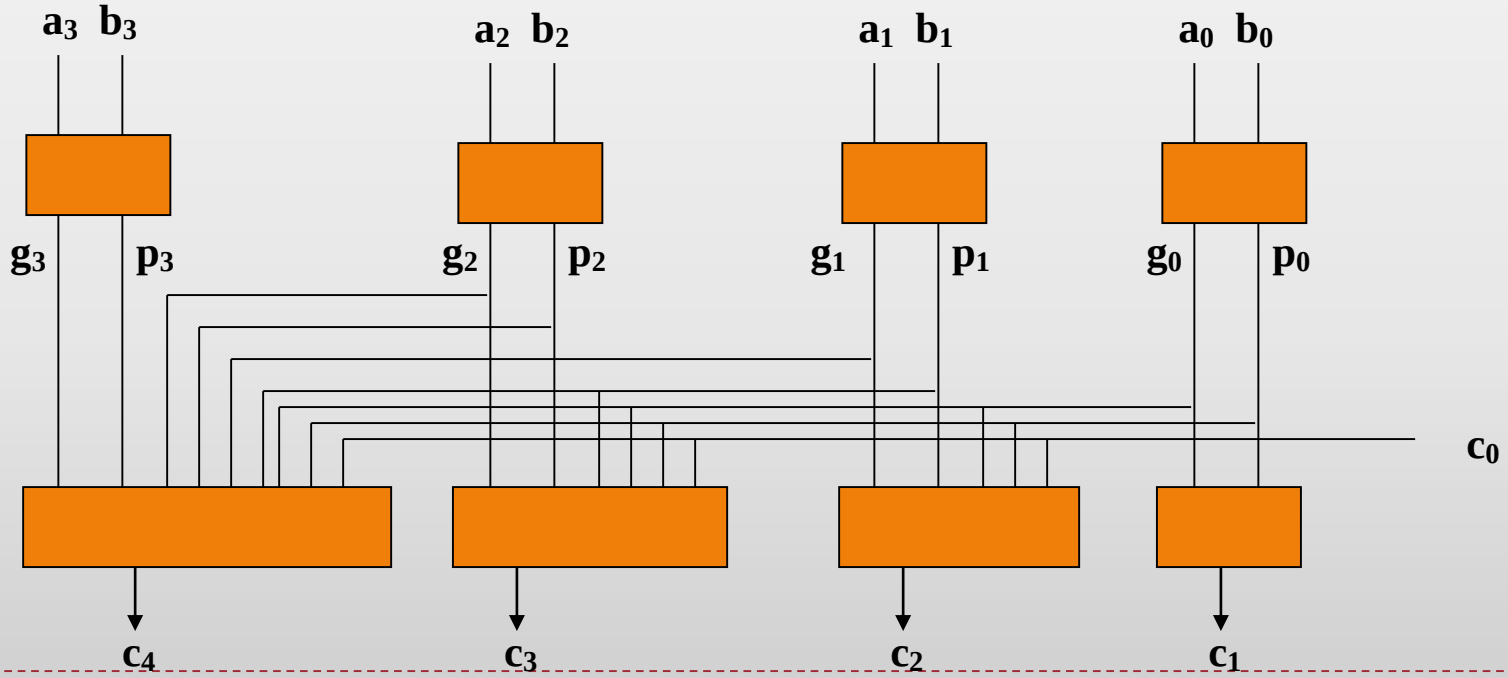
If we consider 4 bits, we have that $c_1$, $c_2$, $c_3$, $c_4$, depend only on $c_0$:

$c_1 = a_0b_0 + (a_0+b_0)c_0 = g_0 + p_0c_0$

$c_2 = a_1b_1 + (a_1+b_1)c_1 = g_1 + p_1c_1 = g_1 + p_1g_0 + p_1p_0c_0$

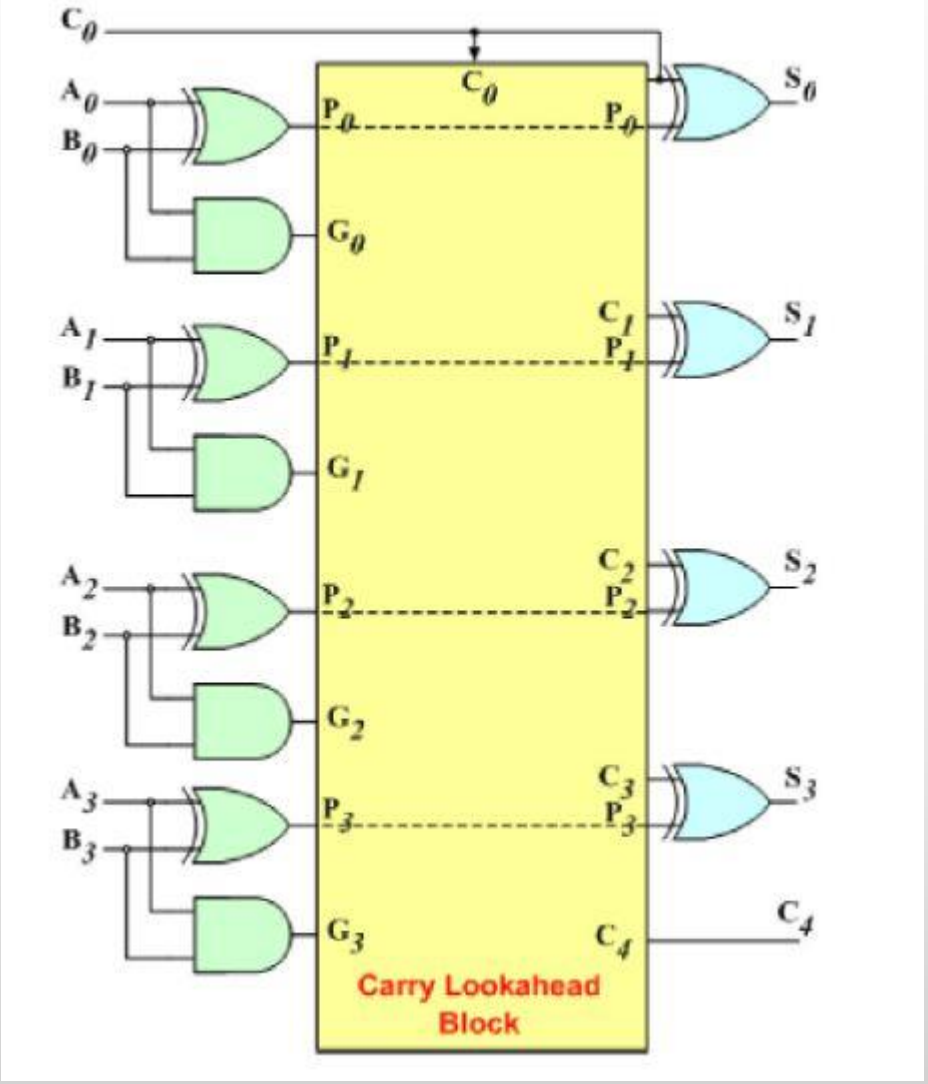
$c_3 = a_2b_2 + (a_2+b_2)c_2 = g_2 + p_2c_2 = g_2 + p_2g_1 + p_2p_1g_0 + p_2p_1p_0c_0$

$c_4 = a_3b_3 + (a_3+b_3)c_3 = g_3 + p_3c_3 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g_0 + p_3p_2p_1p_0c_0$



# Carry-Lookahead Addition

- Structure of a 4 bit CLA
- A CLA requires one logic level to form *p* and *g*, two levels for the carries, and two for the sum, for total of **five logic levels**
- Unfortunately, a carry-lookahead adder on *n* bits requires a fan-in of *n* + 1 at the OR and at the rightmost AND gate



# Carry-Lookahead Adder

If we consider 4 bits, we have that $c_1$, $c_2$, $c_3$, $c_4$, depend only on $c_0$:

- $c_1 = g_0 + p_0c_0$

  $T_{c1} = 2T_{gate}$

  $A_{c1} = 2A_{gate}$
- $c_2 = = g_1 + p_1g_0 + p_1p_0c_0$

  $T_{c2} = 3T_{gate}$

  $A_{c2} = 5A_{gate}$
- $c_3 = g_2 + p_2g_1 + p_2p_1g_0 + p_2p_1p_0c_0$

  $T_{c3} = 4T_{gate}$

  $A_{c3} = 9A_{gate}$
- $c_4 = g_3 + p_3c_3 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g_0 + p_3p_2p_1p_0c_0$

  $T_{c4} = 5T_{gate}$

  $A_{c4} = 14A_{gate}$

# Carry-Lookahead Adder

- If we consider that:

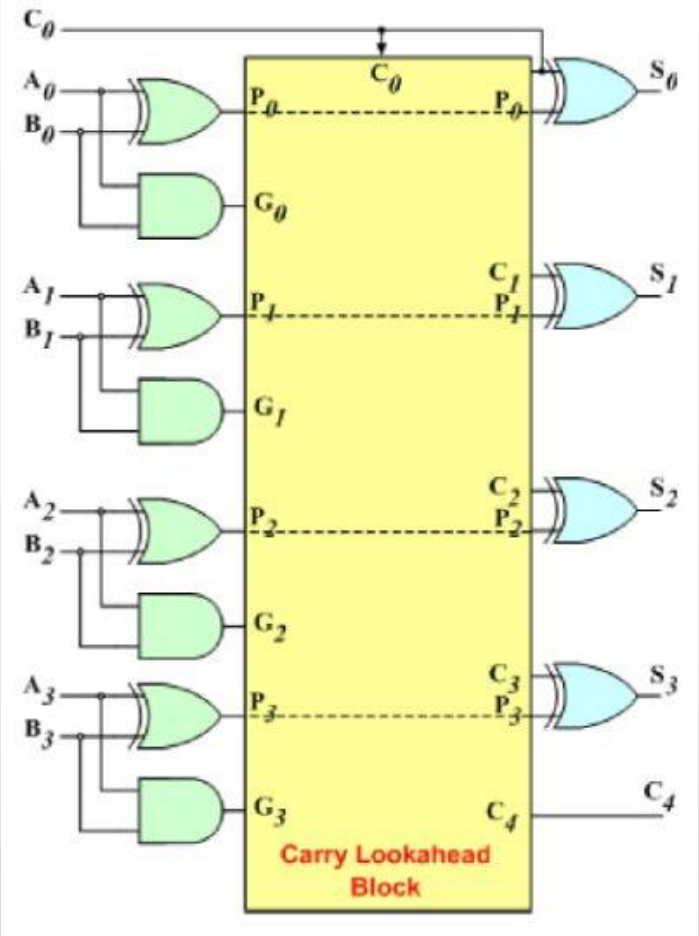
  Carry Generate $g_i = a_i b_i$

  Carry propagate $p_i = a_i \oplus b_i$

  - $T_{gi} = T_{gate}$ and $A_{gi} = A_{gate}$
  - $T_{pi} = 2T_{gate}$ and $A_{pi} = 2A_{gate}$

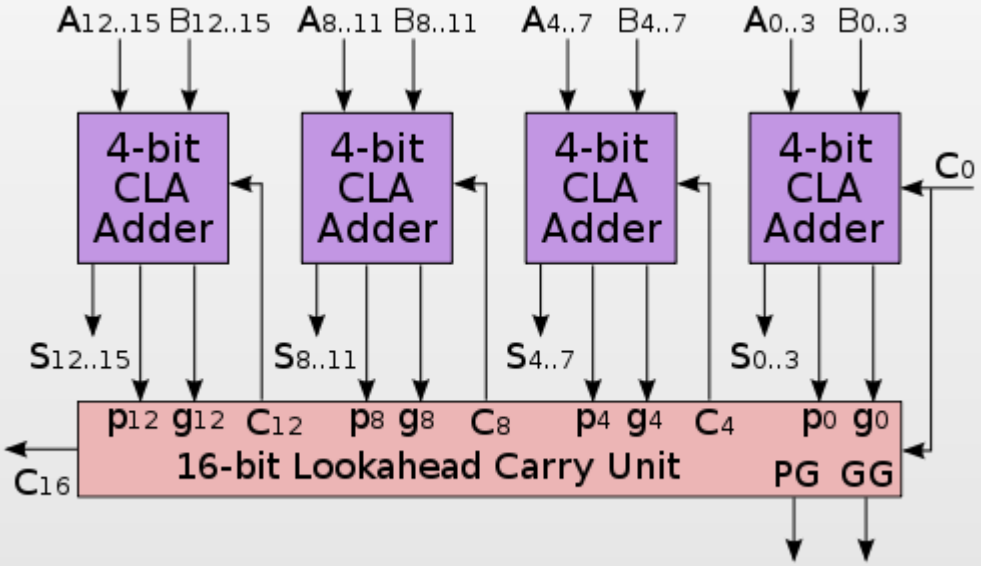
  The total is:

  - $T_{CLA} = 2T_{gate} + 5T_{gate} + 2T_{gate} = 9T_{gate}$
  - $A_{CLA} = 12A_{gate} + 30A_{gate} + 8A_{gate} = 50A_{gate}$



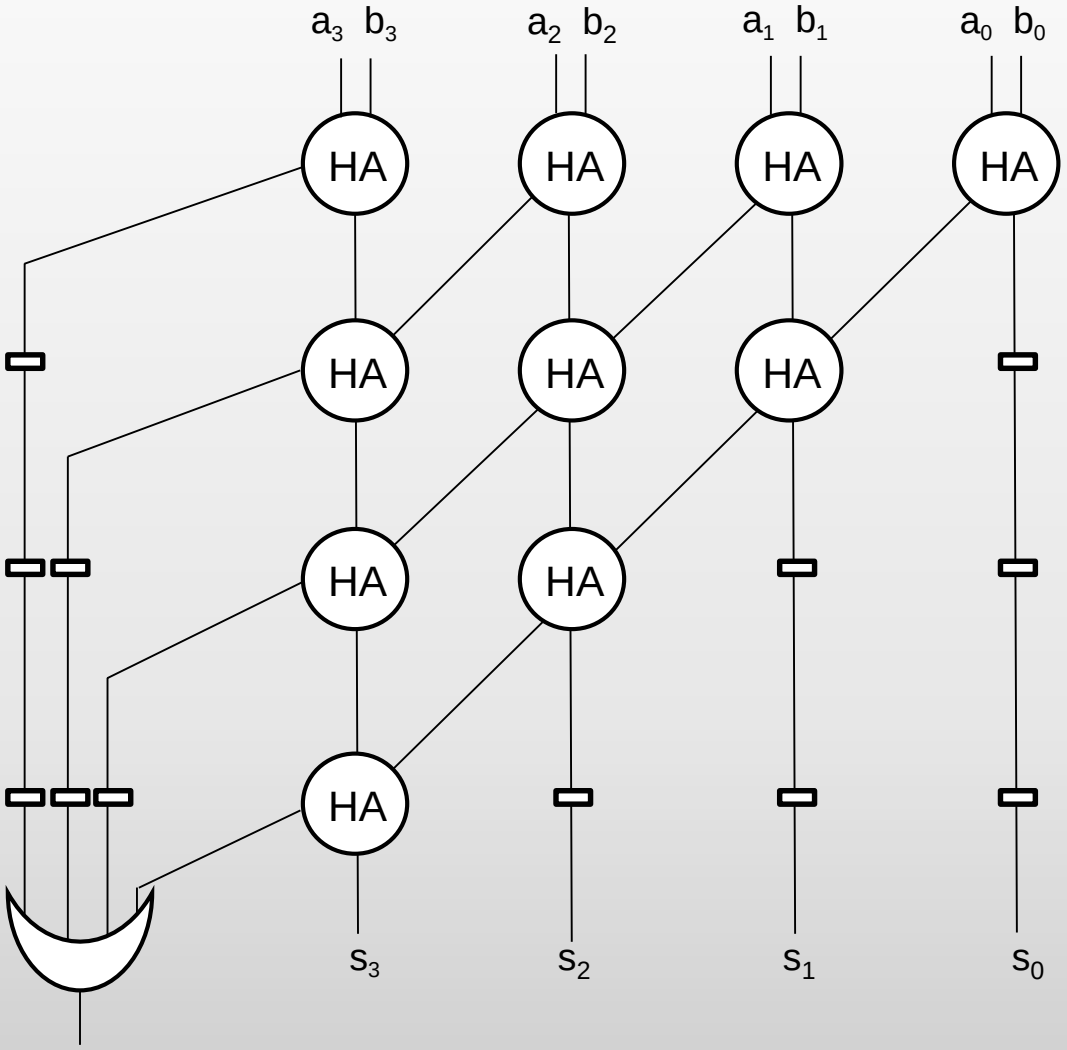
# Carry-Lookahead Addition

- A 16-bit adder can be built from four 4-bit adders, and a 4-bit carry look-ahead unit at the second level

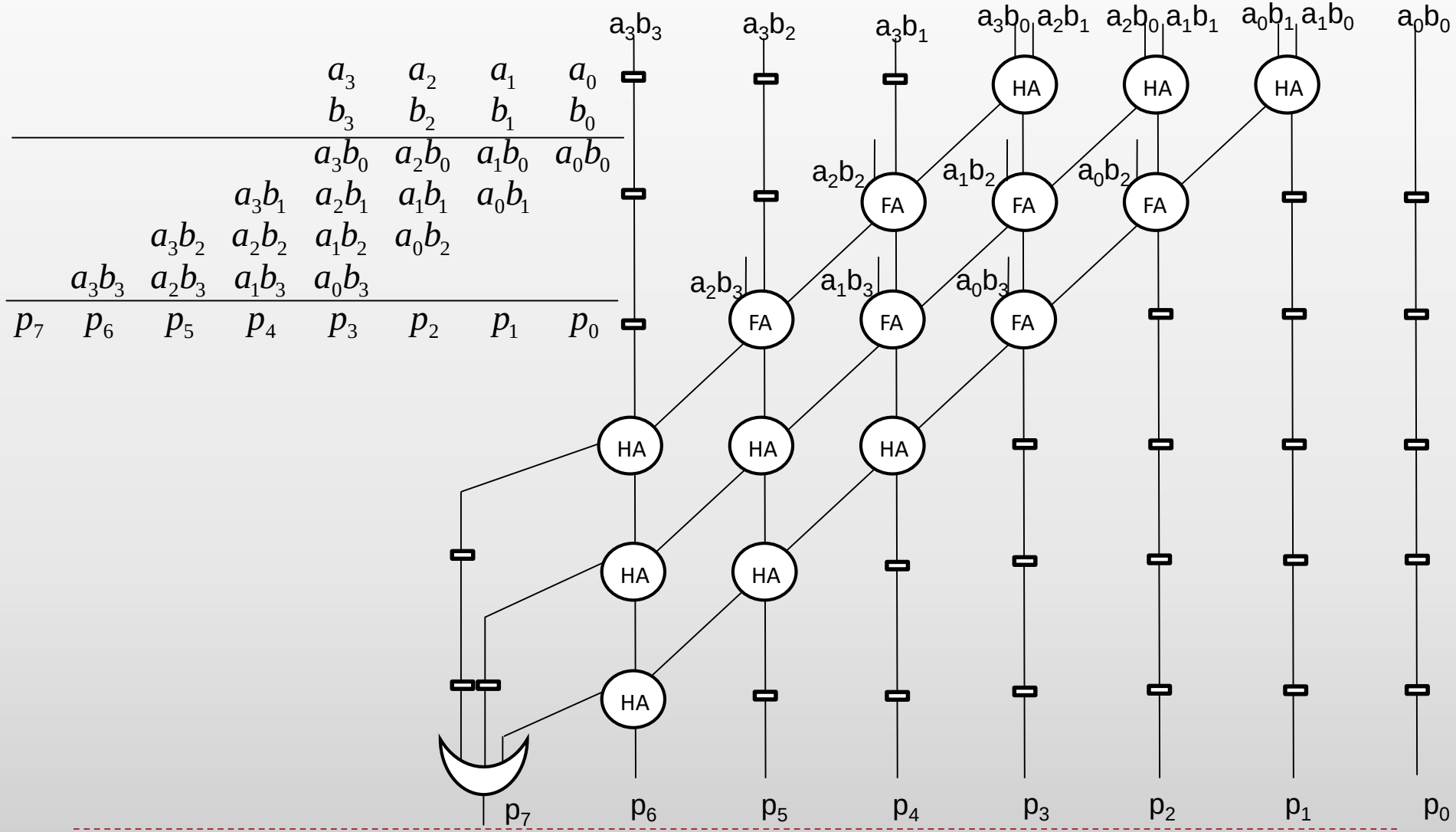



- A 64-bit adder can be built from sixteen 4-bit adders, four 4-bit carry look-ahead units at the second level, and a single 4-bit carry look-ahead unit at the third level

# Pipelined Addition



# Pipelined Unsigned Multiplication



# Pipelined Signed Multiplication

| | | $a_5$ | $a_4$ | $a_3$ | $a_2$ | $a_1$ | $a_0$ |
|---|---|---|---|---|---|---|---|
| | | $b_5$ | $b_4$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ |
| | | $a_5b_0$ | $a_4b_0$ | $a_3b_0$ | $a_2b_0$ | $a_1b_0$ | $a_0b_0$ |
| | $a_5b_1$ | $a_4b_1$ | $a_3b_1$ | $a_2b_1$ | $a_1b_1$ | $a_0b_1$ | |
| $a_5b_2$ | $a_4b_2$ | $a_3b_2$ | $a_2b_2$ | $a_1b_2$ | $a_0b_2$ | | |
| $a_4b_3$ | $a_3b_3$ | $a_2b_3$ | $a_1b_3$ | $a_0b_3$ | | | |
| $a_3b_4$ | $a_2b_4$ | $a_1b_4$ | $a_0b_4$ | | | | |
| $a_2b_5$ | $a_1b_5$ | $a_0b_5$ | | | | | |
| | | $p_5$ | $p_4$ | $p_3$ | $p_2$ | $p_1$ | $p_0$ |